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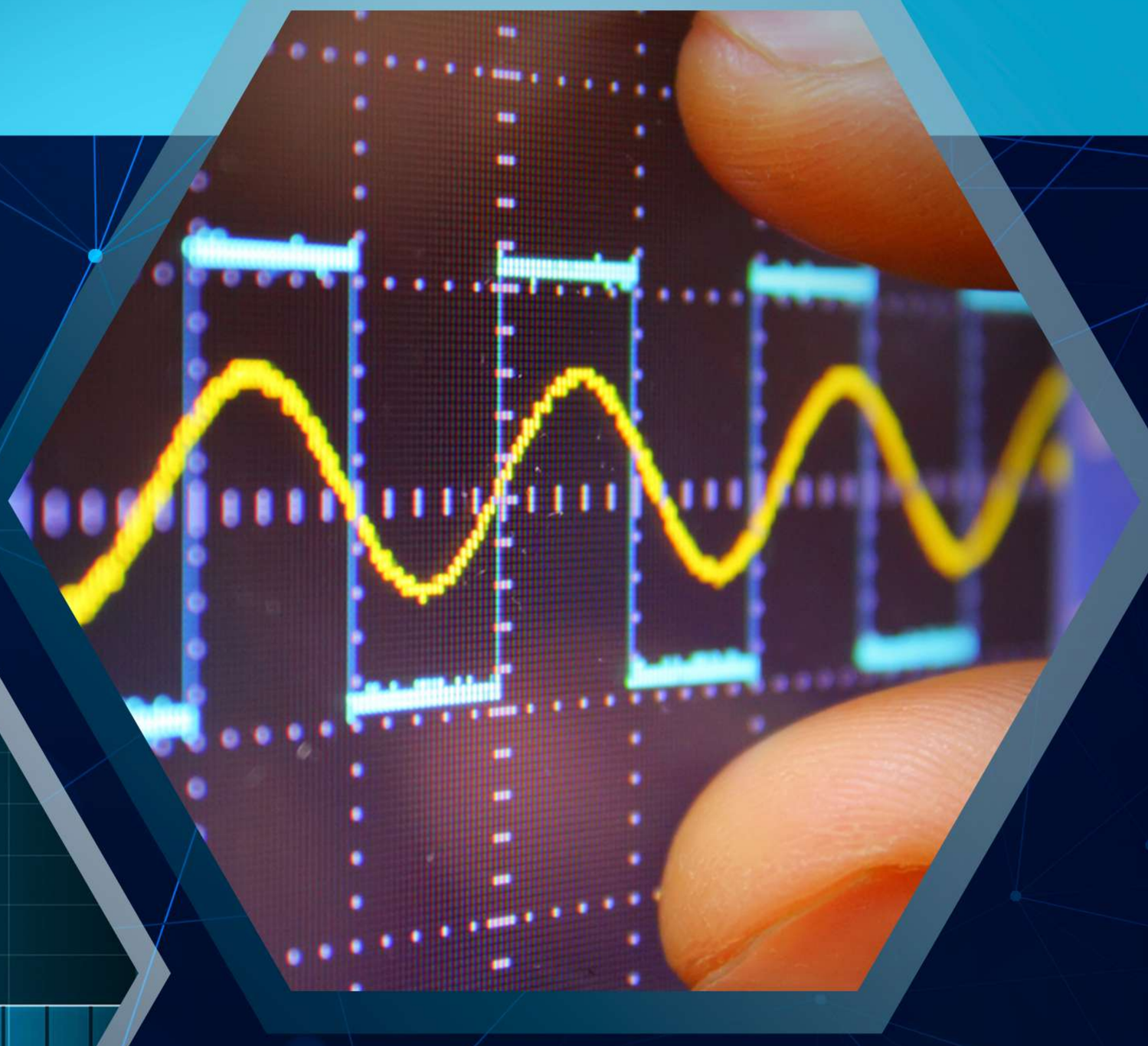

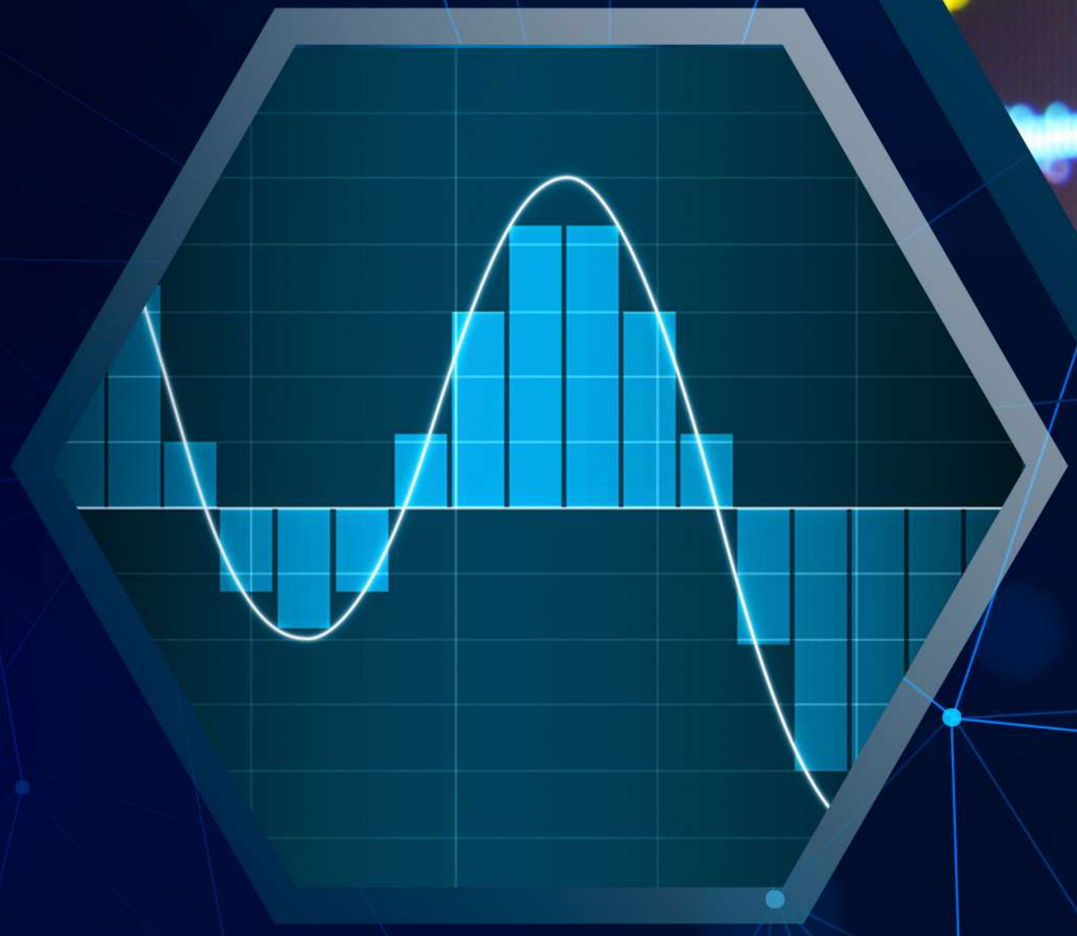

WHITEPAPER

NOISE REDUCTION LESS THAN 100 uVrms ON THE CCD ANALOG VIDEO SIGNAL ACQUISITION

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Contents

Noise reduction less than 100 uVrms on the CCD analog video signal acquisition

1. Digitizer card and digital acquisition hardware specification:

The digitizer card and digital acquisition hardware will be part of analog signal acquisition and processing system. It will interface with Video amplifier board at input, convert analog video output to digital signal and interface to host computer for digital trigger based synchronous acquisition and further processing of data. Analog video output from CCD is a periodic signal (similar to square wave), which can have maximum frequency as defined in table-6a & table-6b. Two options for digitizer card is explored: **Option-1:** AFE based and **Option-2:** non-AFE based.

In option-1, Digitizer card will sample this periodic analog signal at high frequency (minimum 16X analog input frequency) using an ADC so the signal can be effectively reproduced by its digital equivalent values.

Table-6a: Digitizer card and digital acquisition hardware specification requirement for different test benches (Option-1)

Sr. No.	Specifications (Option-1)	TB
1.	No. of independent analog input channels (1 MΩ input impedance, AC and DC coupling)	16
2.	Analog input voltage range (max Pk-Pk, V) (a) setting -1 (b) setting -2 (c) setting -3	 0.2 1-2 4
3.	Maximum analog input frequency (MHz)	12
4.	Digitization (ENOB) @ setting -2	≥10.5 Bits
5.	Minimum external sample clock frequency (MHz)	≥ 16 x analog input frequency
6.	On board memory per channel (MB)	≥ 8
7.	Noise (RMS, % of full-scale analog input range)	≤ 0.06
8.	Data streaming rate to PC	≥ 128MB/s

In option-2, Digitizer card will have analog front end (AFE) with ADC for correlated double sampling (CDS) of analog input signal and digitization of CDS sample.

Table-6b: Digitizer card and digital acquisition hardware specification requirement for different test benches (Option-2)

Sr. No.	Specifications (Option-1)	TB
1.	No. of independent analog input channels (1 MΩ input impedance, AC and DC coupling)	12
2.	Analog input voltage range (max Pk-Pk, V)	2
3.	Maximum analog input frequency (MHz)	12
4.	Digitization minimum	14 Bits
5.	On board memory per channel (MB)	≥ 1
6.	Noise (RMS, % of full-scale analog input range)	≤ 0.007
7.	Data streaming rate to PC	≥ 20MB/s

Digitizer card combined with digital acquisition hardware must have industry standard instrumentation interface like USB 3.0 to host.

Electrical test in this card includes measurement of card specifications.

2. Option 1 Design Approach and noise reduction on CCD video signal

We have design 16 Channel digitizer board with option 1. Digitizer card will sample this periodic analog signal at high frequency (minimum 16X analog input frequency) using an ADC so the signal can be effectively reproduced by its digital equivalent values.

The maximum frequency of signal is 12 MHz. The sampling rate in case of option 1 is 192 MSPS. We will sample the data at 200 MSPS in 2x decimation digital mode of ADC.

Input impedance	Chain Gain(V/V)	Output referred noise @ADC input(uVrms)	Total noise including ADC (uVrms)	Total noise in analog path
50 Ohm	1	230.44	305.1271761	305.1271761
	8	286.3	349.2387292	43.65484115
>1 M Ohm	1	230.31	305.0290086	305.0290086
	8	279.54	343.7187973	42.96484966

Noise quantification of receiver chain

The Chain gain and averaging the samples inside FPGA would results in reduction of noise.

The noise achieved on the CCD video signal will be less than 100uVrms.

3. Option 2 Design Approach and noise reduction on CCD video signal

we have design 12 Channel digitizer board with option 2. Digitizer card will have analog front end (AFE) with ADC for correlated double sampling (CDS) of analog input signal and digitization of CDS sample.

Advantages with Option 2(non AFE based) are:

Correlated double sampling is a method to measure electrical values that allows removing an undesired offset. It is used often when measuring sensor outputs. The output of the sensor is measured twice: once in a known condition and once in an unknown condition. The value measured from the known condition is then subtracted from the unknown condition to generate a value with a known relation to the physical quantity being measured.
This is commonly used in switched capacitor operational amplifiers to effectively double the gain of the charge sharing opamp, while adding an extra phase.
When used in imagers, correlated double sampling is a noise reduction technique in which the reference voltage of the pixel (i.e., the pixel's voltage after it is reset) is subtracted from the signal voltage of the pixel (i.e., the pixel's voltage at the end of integration) at the end of each integration period, to cancel the thermal noise associated with the sensor's capacitance.

Noise achieved on the CCD video signal is less than 300 uVrms

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Thank You!

Does anyone have any questions?

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