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# PCI Express 3.0 Equalization: **THE MYSTERY UNSOLVED**

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# PCI Express 3.0 Equalization: The Mystery Unsolved

## Need of Equalization:

PCI Express (PCIe) Gen 3.0 is the next generation general-purpose I/O interconnect standard. It aims to provide 8GT/s bit rate across the same copper channel, almost doubling the data throughput over PCIe Gen 2.0.

PCIe channels are band-limited in nature and provide quite large signal attenuation at the higher frequencies (22 dB @ 4GHz corresponding to 8GT/s). The high frequency component of PCIe 3.0 signal gets diminished while passing such a band-limited channel. The result is distortion and spreading of the transmitted signal over multiple symbols, generating Inter symbol interference (ISI) and bit errors at the receiver.

## Meaning of Equalization:

PCIe 3.0 specification envisages the provision of performing Equalization at the transmitter and/or at the receiver to mitigate the effect of ISI and hence, to minimize the bit error rate (BER). In Equalization, the signal is passed through a Filter having its frequency response equal to inverse of frequency response of the channel. A high gain is applied at higher frequency to counter the signal attenuation at the high frequencies. In simple words, Equalization is an adaptive filter with coefficients determined on runtime depending upon the physical channel.

Equalization can be performed either at transmitter side and/or at receiver side. The received signal is mixed with the channel noise, hence Equalization at the receiver side may cause noise enhancement and degrade Signal to Noise (SNR) ratio. However, the equalization at the transmitter side is free from the noise enhancement problem. Thus the Equalization at the transmitter side is more effective.

## PCIe 3.0 Equalization:

Equalization at transmitter side (TxEQ) is based on a simple 3-tap FIR filter as shown in Figure 3. Three consecutive received pulses ( $v_{inn-1}$ ,  $v_{inn}$ , and  $v_{inn+1}$ ) are multiplied with three different filter coefficients ( $c_{-1}$ ,  $c_0$ , and  $c_{+1}$ ) and then multiplier outputs are added together to produce the final filter output.

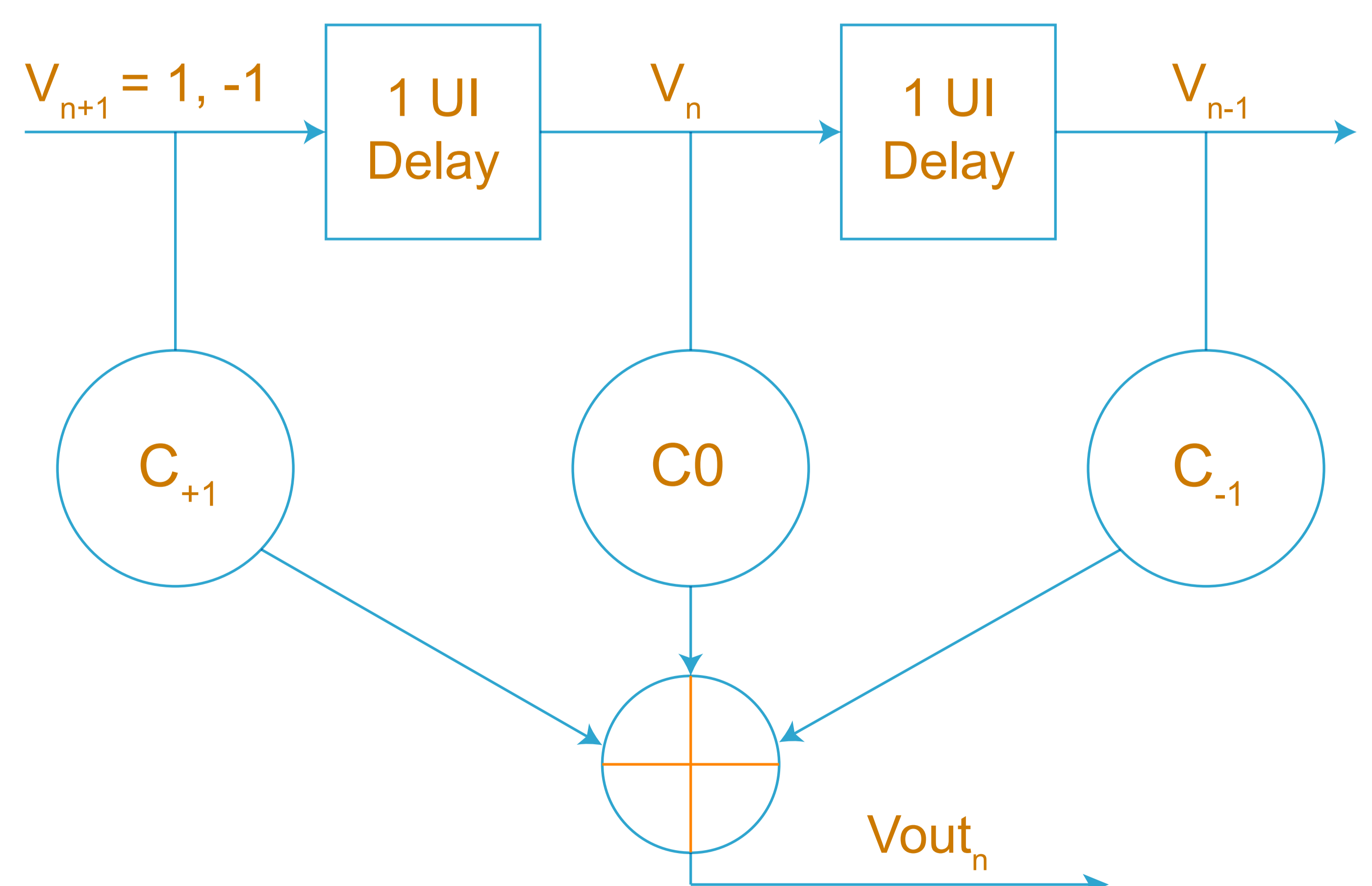


Figure 1: TX Equalization: FIR Filter Representation



$c_{-1}$ ,  $c_0$ , and  $c_{+1}$  are known as the pre-cursor, cursor and post-cursor coefficients, respectively. They are defined in such a way that  $c_0 > 0$ ,  $c_{-1} \leq 0$ ,  $c_{+1} \leq 0$ . The value of these coefficients is subjected to some protocol defined constraints, which we will discuss later in this document.

The 3-tap FIR filter output is given following eq.

$$v\_out_n = v\_in_{n-1} * c_{-1} + v\_in_n * c_0 + v\_in_{n+1} * c_{+1} \dots (1a)$$

OR

$$v\_out_n = -v\_in_{n-1} * |c_{-1}| + v\_in_n * |c_0| - v\_in_{n+1} * |c_{+1}| \dots (1b)$$

The transmitter may either use the default value of these coefficients from its registers, or may use the values communicated to it by the receiver in TS1/TS2 symbols during some protocol defined Link Training and Status State Machine (LTSSM) states. More detail is given ahead in this document.

## De-emphasis and Pre-shoot

Fig. 2 show the resultant output signal when a binary input stream is applied to a 3-tap FIR Filter. It can be seen that the output takes a different value just before and after polarity inversion of the input bit stream. PCIe 3.0 specification defines new terminologies corresponding to these events as explained in Table 1. Voltages  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  correspond to De-emphasis, Flat level, Pre-shoot and Maximum-boost events, respectively.

PCIe 3.0 Term	Corresponding Condition on Input Signal
Flat Level	A constant voltage will appear when bits of same polarity are being transmitted (Refer to $V_b$ in Fig. 2)
Pre-shoot	A boost appears just before the polarity inversion (Refer to $V_c$ in Fig. 2)
Maximum Boost	A major boost appears when there is polarity inversion only for one bit interval (Refer to $V_d$ in Fig. 2)
De-emphasis	A boost appears just after the polarity inversion (Refer to $V_a$ in Fig. 2)

Table 1: Different Equalization Terminologies

Amount of boost is quantified (in dB) with the help of following equations.

$$De - emphasis = -20 \log_{10} \frac{V_a}{V_b} \dots (2a)$$

$$Preshoot = 20 \log_{10} \frac{V_c}{V_b} \dots (2b)$$

$$Maximum boost = 20 \log_{10} \frac{V_d}{V_b} \dots (2c)$$

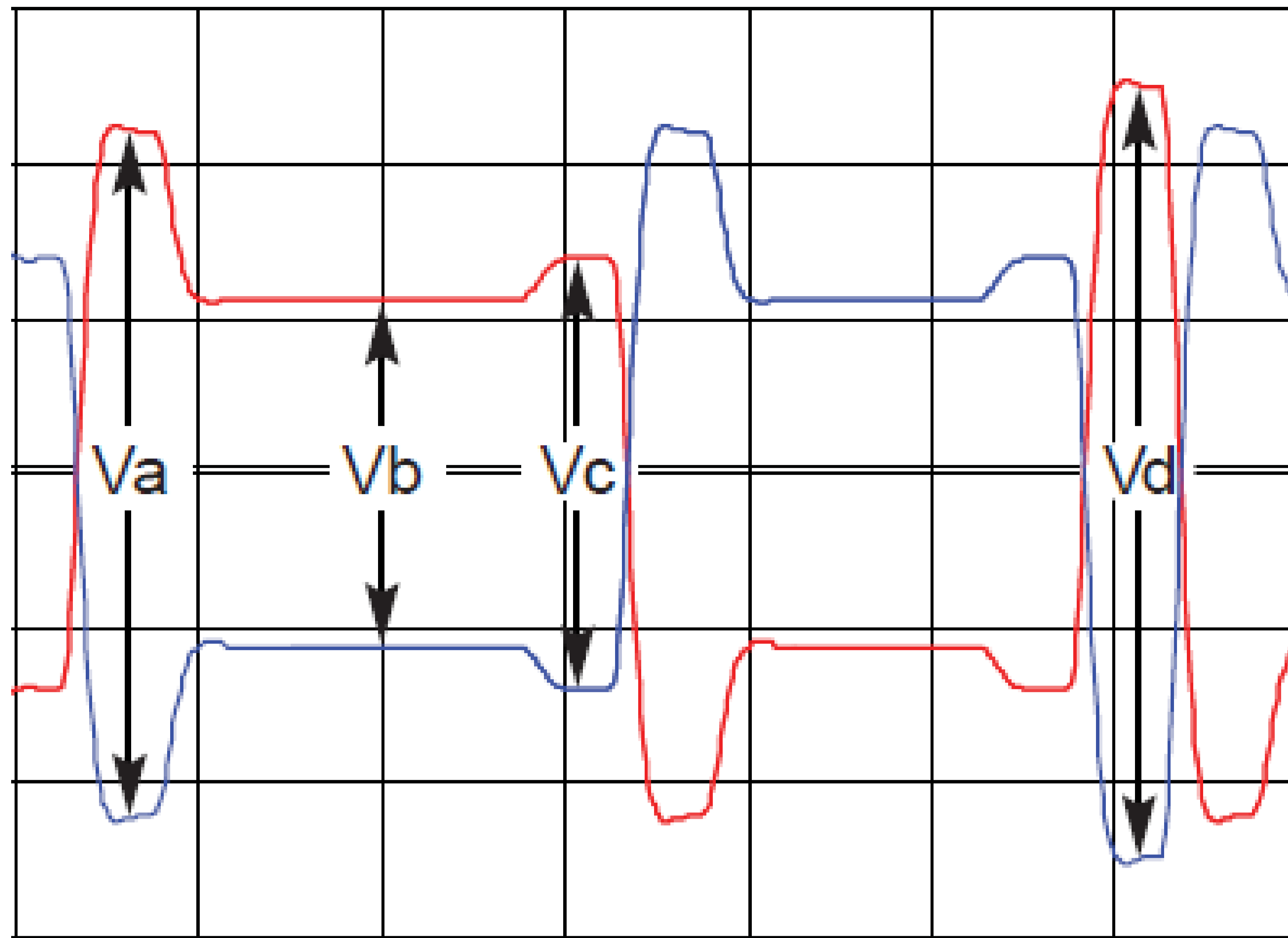


Figure 2: De-emphasis and Pre-shoot

## Coefficients

PCIe 3.0 spec defines two new parameter Full Swing (FS) and Low Frequency (LF) to specify the transmitter voltage characteristics.

1. The maximum differential voltage that can be generated by the transmitter is indicated by FS. To keep the output transmitted power constant with respect to coefficients, sum of absolute value of the coefficients should be equal to FS.

$$FS = |c_0| + |c_{-1}| + |c_{+1}| \dots \dots \dots (3a)$$

2. The minimum differential voltage that can be generated by the transmitter is indicated by LF. The Flat level voltage should always be greater than minimum differential voltage.

$$c_0 - |c_{-1}| - |c_{+1}| \geq LF \dots \dots \dots (3b)$$

3. The specification also sets an upper limit on the allowed Pre-shoot.

$$|c_{-1}| \leq LF/4 \dots \dots \dots (3c)$$

## Presets

PCIe 3.0 specification specifies some predefined set of values of all the three Coefficients which are referred to as Presets. The encoding for the Transmitter presets is provided in Table 2.



Preset No.	De-emphasis (dB)	Pre-shoot (dB)	$C_{-1}$	$C_0$	$C_{+1}$
P0	-6	0	0.000	0.750	-0.250
P1	-3.5	0	0.000	0.833	-0.167
P2	-4.4	0	0.000	0.800	-0.200
P3	-2.5	0	0.000	0.875	-0.125
P4	0	0	0.000	1.000	0.000
P5	0	1.9	-0.100	0.900	0.000
P6	0	2.5	-0.125	0.875	0.000
P7	-6	3.5	-0.100	0.700	-0.200
P8	-3.5	3.5	-0.125	0.750	-0.125
P9	0	3.5	-0.167	0.833	0.000
P10	See Note-1 below				
P11-15	Reserved for Later Use.				

*Table 2: TX Preset Ratios and Corresponding Coefficient Values*

*Note 1: Preset P10 corresponds to coefficients value when Flat voltage level is equal to minimum differential voltage. This case will happen when  $C_{-1} = 0$ ,  $C_{+1} = \frac{FS+LF}{2}$ ,  $C_{-1} = \frac{FS-LF}{2}$ , so that eq. 2b above is equal to LF.*

## PCIe 3.0 Equalization Procedure

PCIe 3.0 specification specifies an adaptive mechanism to determine the optimum value of the TxEQ coefficients and presets depending upon the channel behavior.

As a transmitter does not know the channel parameters, the TxEQ coefficients and presets are computed at the receiver side using the received signal. Then these coefficients and presets are communicated to the transmitter using the TS1/TS2 symbols during a protocol defined LTSSM states. The transmitter then applies the received coefficients to the transmitter set-up. This process of computing the coefficients and then communicating them to the transmitter is repeated multiple times until the required BER is achieved.

According to PCIe 3.0 specification, the Equalization procedure must be executed during the first data-rate change to 8.0 GT/s. Components must store their Transmitter set-up that was agreed to during equalization procedure and use it for future operation at 8.0 GT/s data rate.



The equalization procedure can be initiated either autonomously or by software. The autonomous mechanism is executed if both components advertise that they are capable of 8.0 GT/s data rate (via the TS1 and TS2 Ordered Sets) during the initial Link negotiation (when Link-Up is set to 1b). The Downstream Port is required to make the transition from L0 to Recovery to change the data rate to 8.0 GT/s and perform the equalization procedure.

Software can initiate equalization procedure by writing 1b to the Perform Equalization bit in the Link Control 3 register (present in Secondary PCI Express Extended Capability), followed by a write to the Target Link Speed field in the Link Control 2 register to enable the Link to run at 8.0 GT/s, followed by a write of 1b to the Retrain Link bit in the Link Control register of the Downstream Port to perform equalization.

Equalization procedure should not be repeated under normal operating conditions, although there is a provision to repeat the equalization procedure if a Port detects problems with its equalization setting at any time. A Downstream Port may perform equalization again based on its own needs or based on the request from the Upstream Port in the received EQ-TS2 symbols during the Recovery.RcvrCfg sub-state.

The PCIe 3.0 Equalization is divided in 4 different phases (Phase 0 to Phase 3). Phase 2 and Phase 3 are optional and may be executed if there is a requirement to fine-tune the coefficients and/or presets to achieve the required BER. Different Equalization Phases will be described later in this document.

## Equalization Procedure: State Machine Transition

When Equalization is requested by a device, it transitions through Recovery.RcvrLock sub-state to proceed to L0 state at 8GT/s, as shown in Fig. 3 (steps 1 to 8).

In Recovery.RcvrLock sub-state, each device transmits TS1 Ordered Sets with speed-change bit set. For both the devices, next state is Recovery.RcvrCfg after receiving 8 TS1 OS (Step-1).

In Recovery.RcvrCfg sub-state the Downstream Port sends EQ TS2 with valid Transmitter Preset and Receiver Preset hint fields. These Preset values are derived from the Upstream Port's Equalization Control Register (Present in Secondary PCIe Extended Capability). The Upstream Port sends normal TS2 OS. It also stores the Preset values it received in EQ TS2 OS from the downstream port to use them in Equalization Phase0.

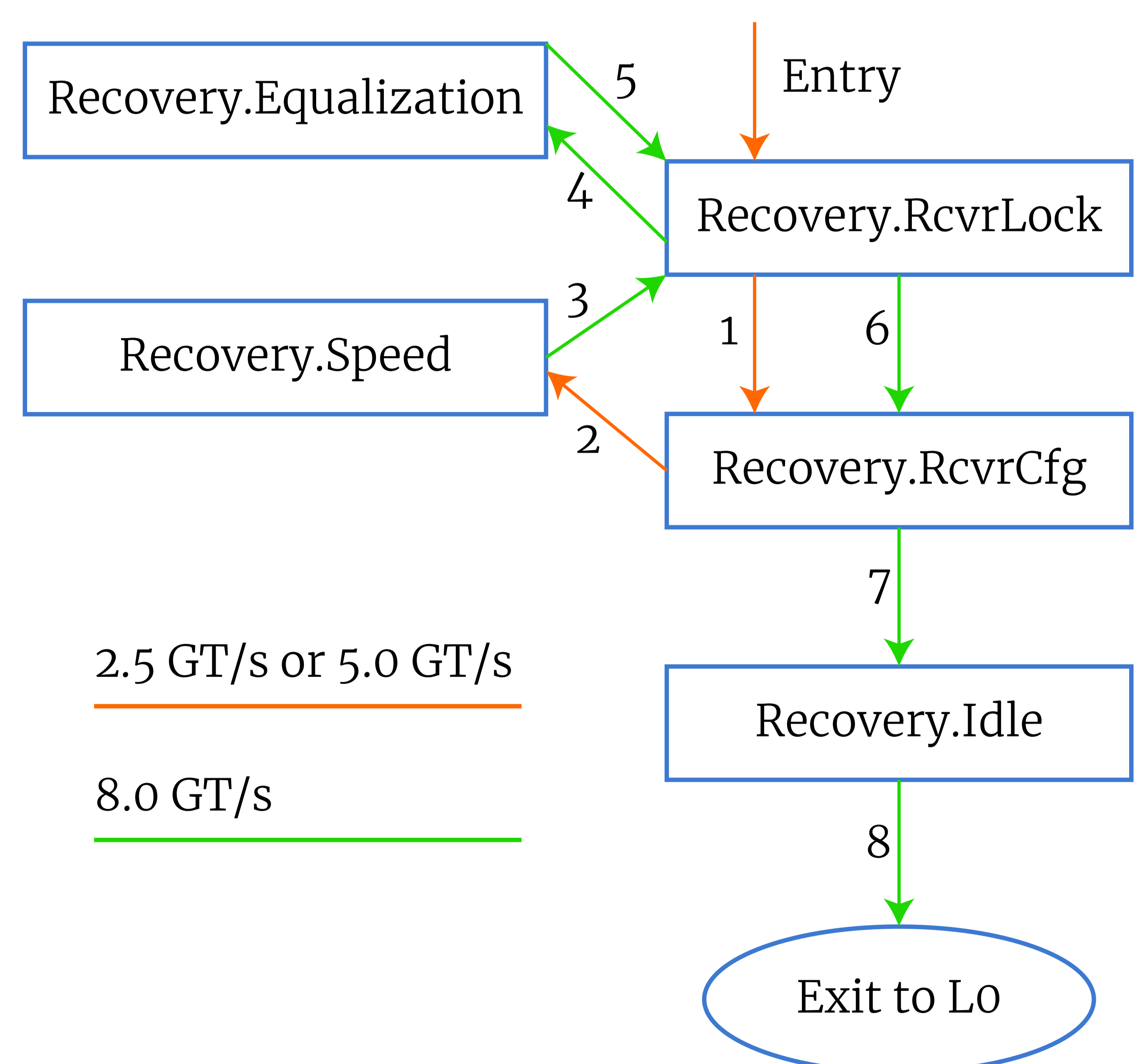


Figure 3: Equalization State Machine Transitions



The next state is Recovery.Speed after receiving 8 TS2 OS (step-2).

In Recovery.Speed sub-state, both devices transmit EIOS OS and then enter into electrical idle where they change to the new speed (8 GT/s) and then transition to Recovery.RcvrLock sub-state again (step-3).

Recovery.RcvrLock is a bypass state for the Downstream Port and it directly goes into Recovery.Equalization Phase 1. The Upstream Port transmits TS1 OS in Recovery.RcvrLock state and it transitions to Recovery.Equalization Phase 0 after receiving TS1 OS with Equalization Command bit (Symbol 6, bit 7) set (step-4).

In Recovery.Equalization sub-state, the Downstream Port starts directly from Phase 1 and Upstream Port starts from Phase 0. Then both devices proceed to Phase 3 to transition to Recovery.RcvrLock sub-state (step-5).

Both devices then transition through Recovery.RcvrLock, Recovery.RcvrCfg, Recovery.Idle sub-states to reach L0 state in a normal manner (steps 6, 7, and 8).

## Different Phases

The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field (Symbol 6, Bit 1:0) in the TS1 Ordered Sets. Please refer to Tables 3 and 4 while reading this section.

### Phase 0:

The Upstream Port transmits TS1 Ordered Sets with EC = 01b (Symbol 6, bits 1:0) and Preset value (Symbol 6, bit 6:3) it received in EQTS2 symbols from Downstream Port during Recovery.RcvrCfg sub-state. This Phase is not applicable for the Downstream Port; it directly starts with Phase 1.

### Phase 0:

In this Phase, both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs.

In this Phase, both components advertise their FS and LF values in the respective TS1 fields [FS (Symbol 7, bits 5:0) & LF (Symbol 8, bits 5:0)].

The Downstream Port first enters into Phase 1 and starts transmitting TS1 Ordered Sets with EC = 01b and using the Preset values from each Lane's Equalization Control Register (Part of Secondary PCI Express Extended Capability).



After receiving these TS1 OS with EC = 01b, the Upstream Port transitions to Phase 1, where it continues to transmit the same Preset values it was transmitting in Phase 0.

The Downstream Port, after receiving these TS1 OS with EC = 01, transitions to Phase 2.

## Phase 2:

In this Phase, the Upstream Port helps the Downstream Port to fine tune its transmitter equalization setting (Preset/Coefficient) until a BER of less than  $10^{-12}$  is achieved on all downstream lanes. Multiple iterations may be performed to achieve the optimum equalization settings.

The Downstream Port first enters into Phase 2 and transmits TS1 Ordered Sets with EC=10b. For the first iteration, the Preset values are kept same as in Phase 1. For the sub-sequent iterations, Presets/Coefficient values are same as in the Preset/Coefficient change request it received from the Upstream Port in this Phase.

Use\_Preset field (Symbol 6, bit 7) is used to identify whether the current request is to change the Preset or the Coefficients.

If Use\_Preset = 1, then the current request is for the Preset change and the requested Preset is reflected in the appropriate field (Symbol 6, bits 6:3).

If Use\_Preset = 0, then the current request is for the Coefficient change and the requested Preset is reflected in the appropriate fields [Pre-Cursor (Symbol 7, bits 5:0), Cursor (Symbol 8, bits 5:0), Post-Cursor (Symbol 9, bits 5:0)].

The Upstream Port evaluates the received TS1 OS and may request the Port on the other side of the link to change Preset or Coefficients.

The entire process of requesting a different Preset or coefficients and evaluating the received TS1 OS is repeated until the Upstream Port is satisfied that the required BER is achieved on the downstream lanes. Then the Upstream Port transitions to the next Phase (Phase 3).

## Phase 3:

This Phase is similar to Phase 2 except the difference that the roles of the Downstream and Upstream Ports are interchanged. In this Phase, the Downstream Port helps the Upstream Port to fine tune its transmitter equalization setting (Preset/Coefficient) until a BER of less than  $10^{-12}$  is achieved on all upstream lanes.



## Relevant Training Sequence Fields

In Table 3 and Table 4, we have summarized the equalization related Training Sequence Fields.

Symbol No.	Description
EQTS1- Symbol 6	Bit 2:0 - Receiver Preset Hint. Bit 6:3 - Transmitter Preset. Bit 7 - Set to 1b for EQTS1 symbol.
EQTS2- Symbol 6	Bit 2:0 - Receiver Preset Hint. Bit 6:3 - Transmitter Preset. Bit 7 - Equalization Command.

*Table 3: Relevant Equalization Fields when Operating Speed is 2.5 GT/s or 5.0 GT/s*

Symbol No.	Description
TS1- Symbol 6	Bit 1:0 – Equalization Control (EC). This field refers to the Equalization Phase which is currently being executed.
	Bit 2 – Reset EIEOS Interval Count
	Bit 6:3 – Transmitter Preset. (See note-1)
	Bit 7 – Use Preset. This bit is set means that the Port is initiating a Preset change request (during Phase 3 for Downstream Port or Phase 2 for Upstream Port). If this bit is clear then it is a request for Coefficient change.
TS1- Symbol 7	Bit 5:0 – FS/Pre-Cursor Coefficient (See note-2) For Equalization Phase 1, this field refers to the Full Swing (FS) value. For all other Phases, this field refers to the Pre-Cursor Coefficient. (See note-2)
TS1- Symbol 8	Bit 5:0 – LF/Cursor Coefficient (See note-2) For Equalization Phase 1, this field refers to the Low Frequency (LF) value. For all other Phases, this field refers to the Cursor Coefficient. (See note-2)
TS1- Symbol 9	Bit 5:0 – Post-Cursor Coefficient (See note-2) Bit 6 – Reject Coefficient bit: If the request for change of Preset/Coefficients is not a valid request (i.e. an unsupported/reserved Preset, or the Coefficient which violate one of the rules given by eq.2), then the link-partner must set this bit in the TS1 OS it transmits.

*Table 4: Relevant Equalization Fields when Operating Speed is 8.0 GT/s*



Note-1: For some Equalization Phases (Phase 1 for Downstream port and Phase 0 and Phase 1 for Upstream Port), this field refers to the Preset which is being actually used by the Transmitter in its transmitting lanes. For some Equalization Phases (Phase 3 for Downstream Port and Phase 2 for Upstream Port), if Use\_Preset = 1, this field refers to Preset which this Port is requesting the Port on the other side of the link to change.

For some Equalization Phases (Phase 2 for Downstream port and phase 3 for Upstream port), if Use\_Preset = 1, this field is used to acknowledge the request for change of Preset by the other Port by reflecting the requesting Preset in this field.

Note-2: For some Equalization Phases (Phase 0 for Upstream Port), these field refers to the Coefficients values corresponding to Preset which is being actually used by the Transmitter in its transmitting lanes.

For some Equalization Phases (Phase 3 for Downstream Port and Phase 2 for Upstream Port), if Use\_Preset = 0, these field refers to Coefficients values which this Port is requesting the Port on the other side of the link to change. For some Equalization Phases (Phase 2 for Downstream port and phase 3 for Upstream port), if Use\_Preset = 0, this field is used to acknowledge the request for change of Coefficients by the other Port by reflecting the requesting Coefficients in these field.

## Going Ahead: PCIe 4.0

The PCI Express 4.0 standard is expected to arrive around 2015 and promises 16 Giga-transfers per second, double as much as the PCI Express 3.0 standard. PCIe Gen4 is scheduled to appear in products in about four years.

PCI Special Interest Group (PCI-SIG) has announced that PCIe 4.0 will probably be using the same copper links before the anticipated shift to optical interconnects. To support such 16 GT/s, Gen 4 transceivers will need sophisticated equalization techniques such as multi-tap DFE (Decision Feedback Equalization).

## About the Company

Founded in 2009, Logic Fruit Technologies has a highly experienced management team, which is backed by a talented and committed engineering team. Almost all the employees are hand-picked from IITs and NITs. The company is leading its way into the next generation High Speed Serial Protocols (3 Gbps and above) like PCIe, Fibre Channel, USB, 3G-4G wireless protocols, HDMI and so on. The company has worked closely with reputed high tech companies like Agilent Technologies.

The company has gained a high reputation in market in such a short span due to its innovative outsourcing model, uncompromised quality of work and deep domain knowledge. The main goal of the company is to minimize client's overhead and it works on the simple motto "Outsource and Forget". It has a track record of always exceeding the client's expectations.

**For further information, check the website**

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# Thank You!

Does anyone have any questions?

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