



Whitepaper

# Digital Signaling and Their Inter-conversion

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## Need of Inter-conversion

Nowadays we face many ICs which have different interfaces like LVPECL, LVDS, CML, LVCMOS, TTL, HSTL etc. While designing a PCB schematic, interfacing of one IC with another IC with different signalling supported, becomes a hurdle to design the circuit. In this case a designer always look for an ASIC which can act as a bridge between two signalling. A live example is, when an STM1e PHY (78P2351 from Teridian) is interfaced Xilinx 7 series FPGA, both support different differential signaling. 78P2351 supports LVPECL while Xilinx does not support LVPECL but LVDS. This conversion can be done using resistor-capacitor network only instead of going for a chip.

## Single-Ended Signaling

CMOS and TTL signaling are most popular single-ended signaling besides SSTL signaling. CMOS structure is based on CMOS technology and designed using FETs while TTL is based on BJTs. Both are push-pull based signals.

S/N	Signaling	Voltage Range	Comments
1	CMOS	0-5V	Unipolar
2	LVCMOS	0- 3.3, 3.0, 2.5, 1.5, 1.2, 1.0V	Unipolar
3	TTL	0-5V	Unipolar
4	LVTTL	0-3.3V	Unipolar

## Differential Signaling

Differential signaling has many advantage over single-ended like more noise immune, higher speed, lower EMC etc, but it has some disadvantages like lower fan-out, higher power consumption.

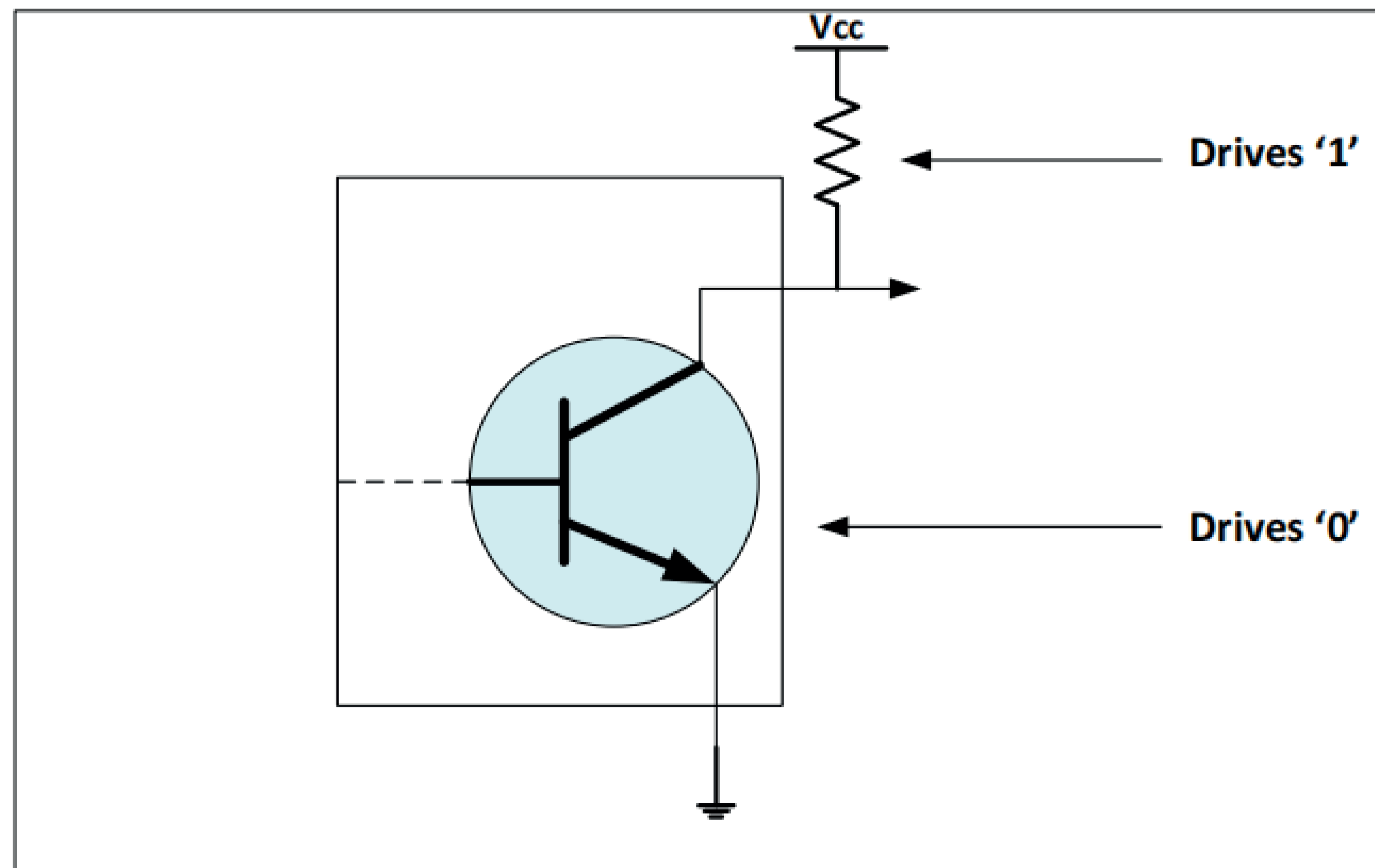
Characteristics of common differential signals is as below

S/N	Signaling	V <sub>cm</sub>	V <sub>pp</sub>
1	LVPECL	2 V	800mV
2	LVDS	1.2 V	400mV
3	CML	1.5	800mV
4	VML	1.25	800mV
5	HSTL	750mV	400mV

# Open-Drain / Open-Collector Architecture

These type of signals are very easy to understand. As Push-pull architecture has capability to make signal high or low by its own, open-drain is able to make only low but not high. When signal is non-zero, it becomes high-Z; this indicates that for receiver to understand the state as non-zero, pull-up is needed which makes it '1' instead of high-Z. These signals do not need level translator as such, as you can choose pull-up voltage which is suitable as per requirement.

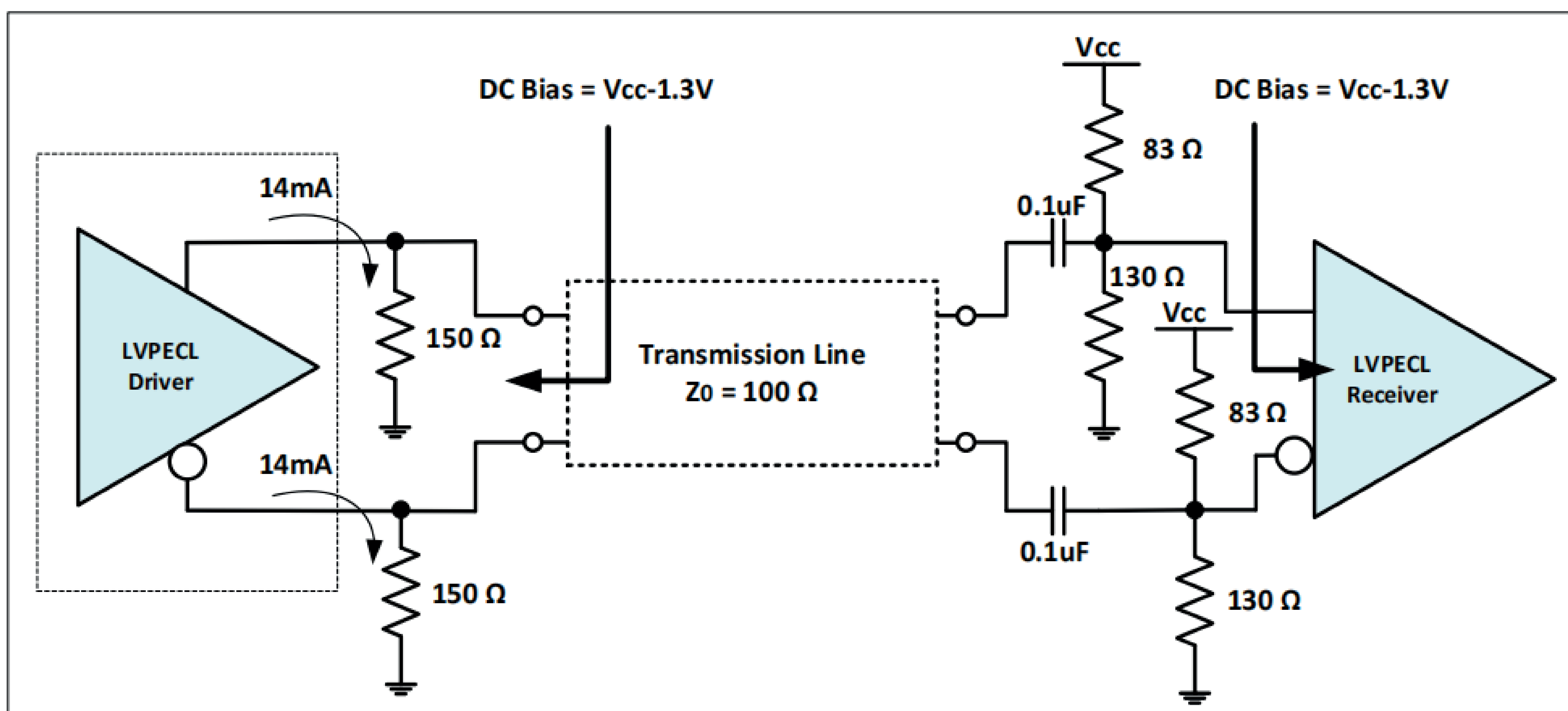
Architecture of open-collector is shown below -



## Differential Logic Families: Inter-conversion

### 1. LVPECL to LVPECL

PECL architecture is made-up of two complimentary BJTs with emitters at output stage. Both P/N pins are current source as internal architecture is emitter-follower. Termination is important to convert the current (typical 14mA) with proper values of resistors. The termination DC bias should be  $V_{cc}-1.3V$  i.e. for  $V_{cc}$  of +3.3V, common mode should come to 2V.



Output is terminated using  $150\Omega$  resistors, which provide output DC bias to  $V_{cc}-1.3V$  ( for  $V_{cc} = +3.3V$ ,  $V_{bias} = 14mA \times 150 = 2.1V \approx 2V = V_{cc}-1.3V$ ). This signal is transmitted over  $100\Omega$  differential transmission line. For LVPECL receiver, common mode will be same as  $V_{cc}-1.3V$ . So, Thévenin Termination is used to provide common-mode voltage as well as  $50\Omega$  load termination on each line.

Common Mode calculation =

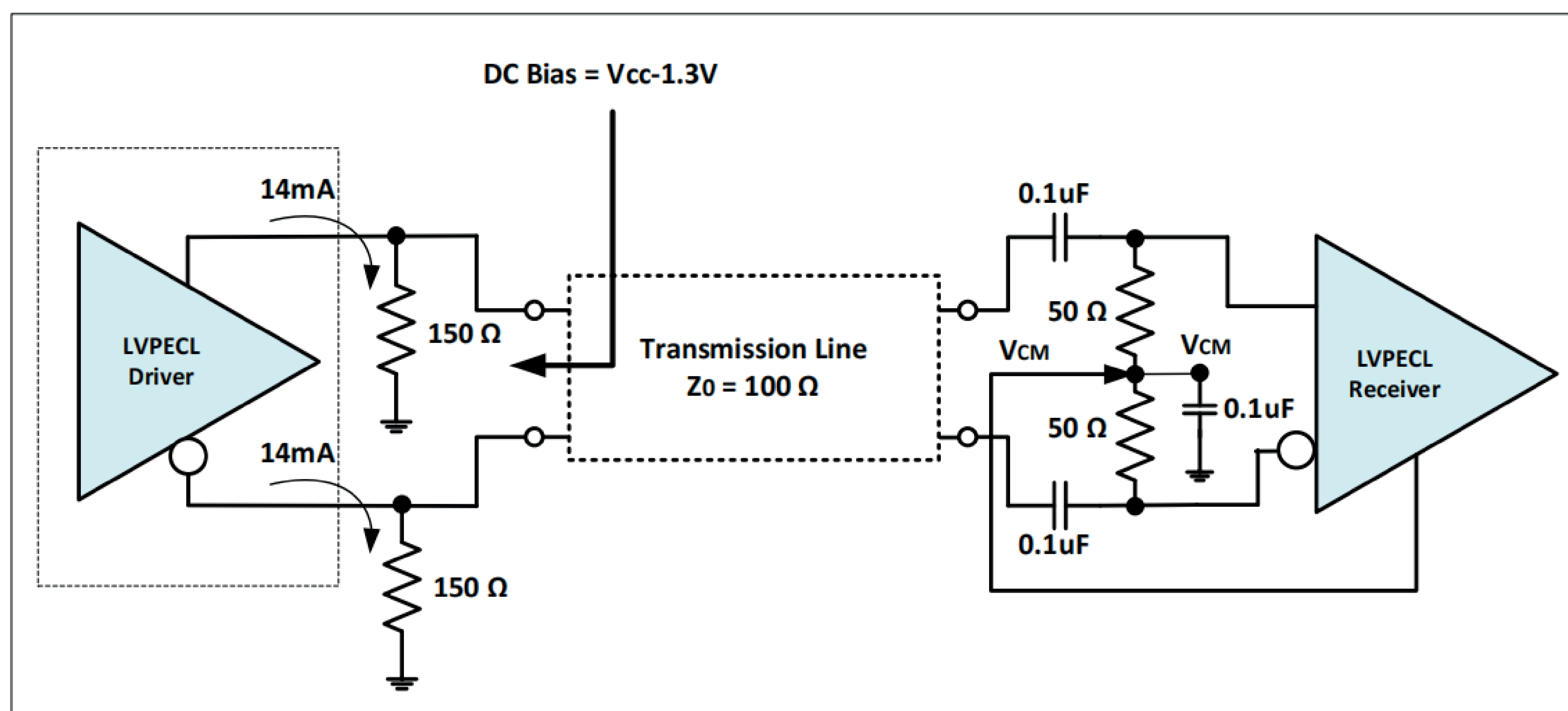
$$V_{cm} = \frac{130}{(130+83)} \times 3.3V = 2.01V = V_{cc}-1.3V$$

Thévenin Termination Calculation for each line =  $R_{th}$

$$R_{th} = \frac{130 \times 83}{(130 + 83)} = 50.6\Omega$$

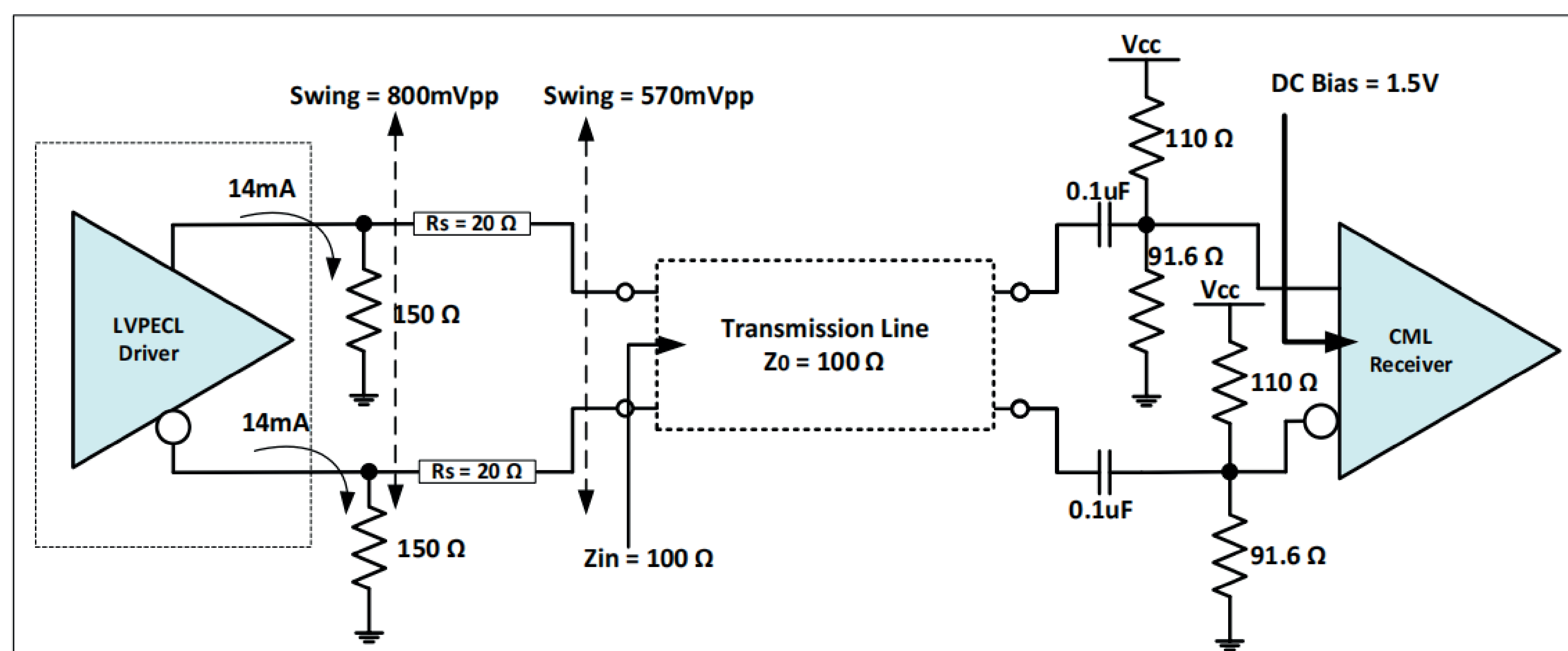
AC-coupling capacitors of  $0.1\mu F$  on each line have been used to remove the common mode voltage of source and other common mode noises that came into transmission line due to its ambience.

Sometimes, receiver itself provide the common mode voltage for the signal to receive. In that case, Thévenin termination is not required as such, so direct  $50\Omega$  is used to terminate and to provide common mode voltage. Its termination is shown below -



## 2. LVPECL to CML Conversion

Similar principal is used LVPECL-to-CML to change the common mode voltage. Here we have option of reducing the swing voltage ( $V_{pp}$ ) according to the capability of receiver.



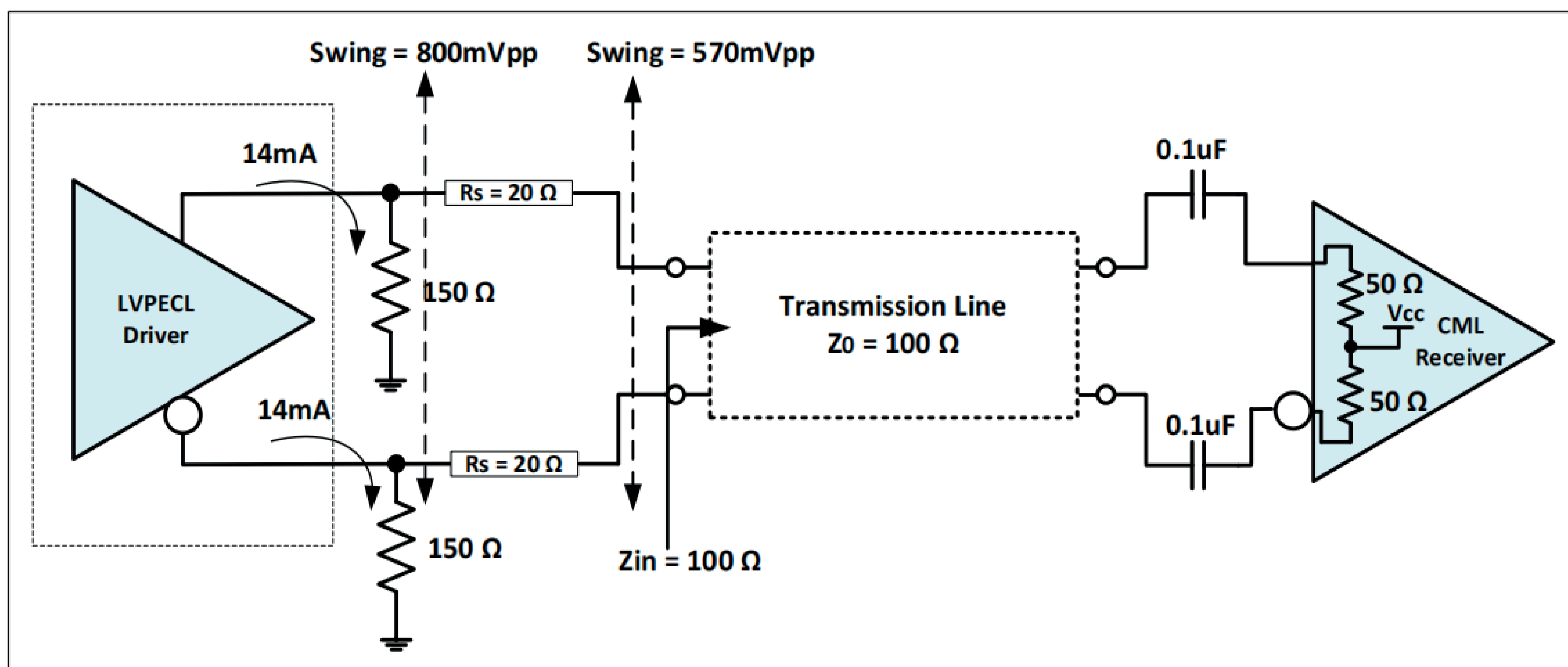
Common Mode calculation for CML =

$$V_{cm} = \frac{91.6}{(91.6+110)} \times 3.3V = 1.5V$$

Thévenin Termination Calculation for each line = Rth

$$R_{th} = \frac{91.6 \times 110}{(91.6 + 110)} = 50\Omega$$

When, CML receiver has its internal termination and common mode, circuit will be as below. This case is used with Xilinx FPGA CML receivers.



Different CML receivers have different swing receiving capability. Maximum value of CLM receiver is 800mVpp. To reduce the Vpp for those receivers which has lower Vpp, a series resistor 'Rs' can be added in series to drop the voltage. Here, example of 20Ω is shown to reduce Vpp from 800mV to 570mV.

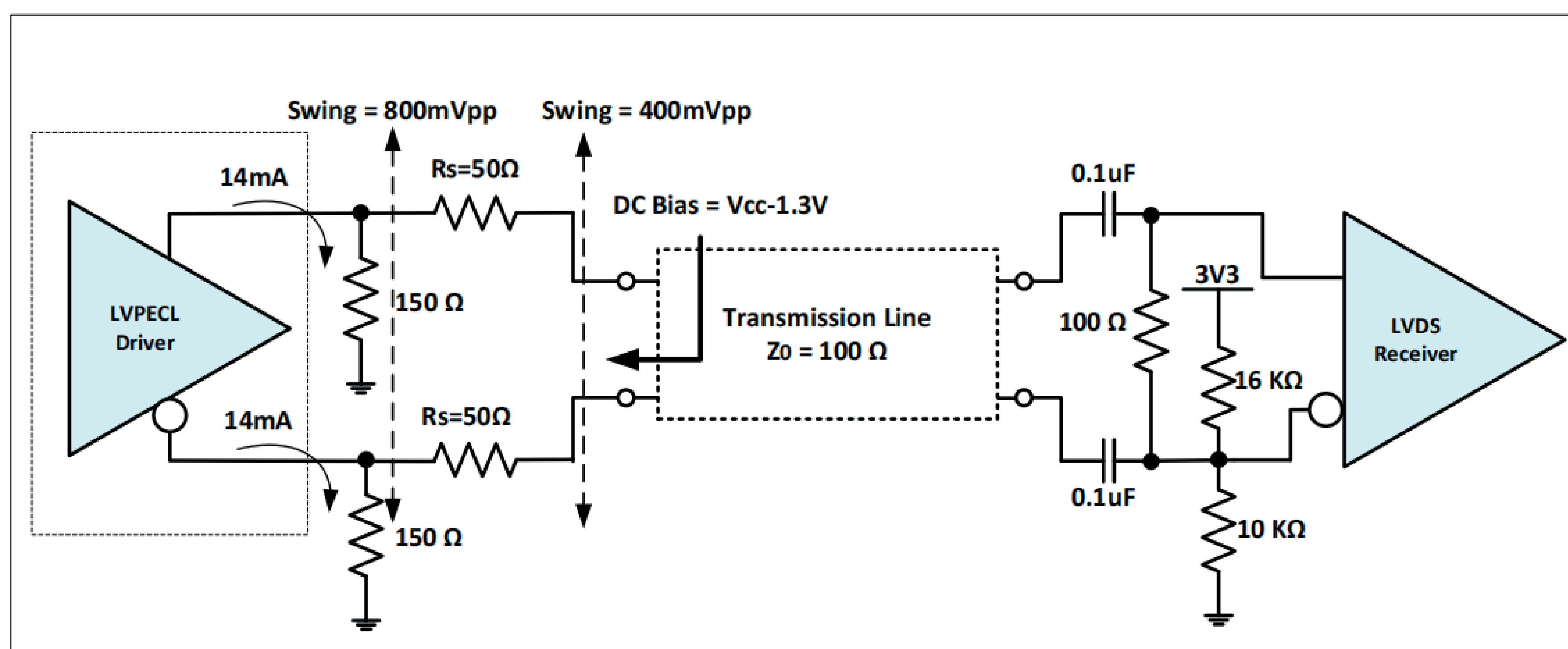
Calculation to change the Vpp at receiver

$$V_{pp}(\text{receiver}) = \frac{Z_{in}}{(Z_{in} + 2 \times R_s)} \times 800$$

$$= 570mV$$

### 3. LVPECL to LVDS Conversion

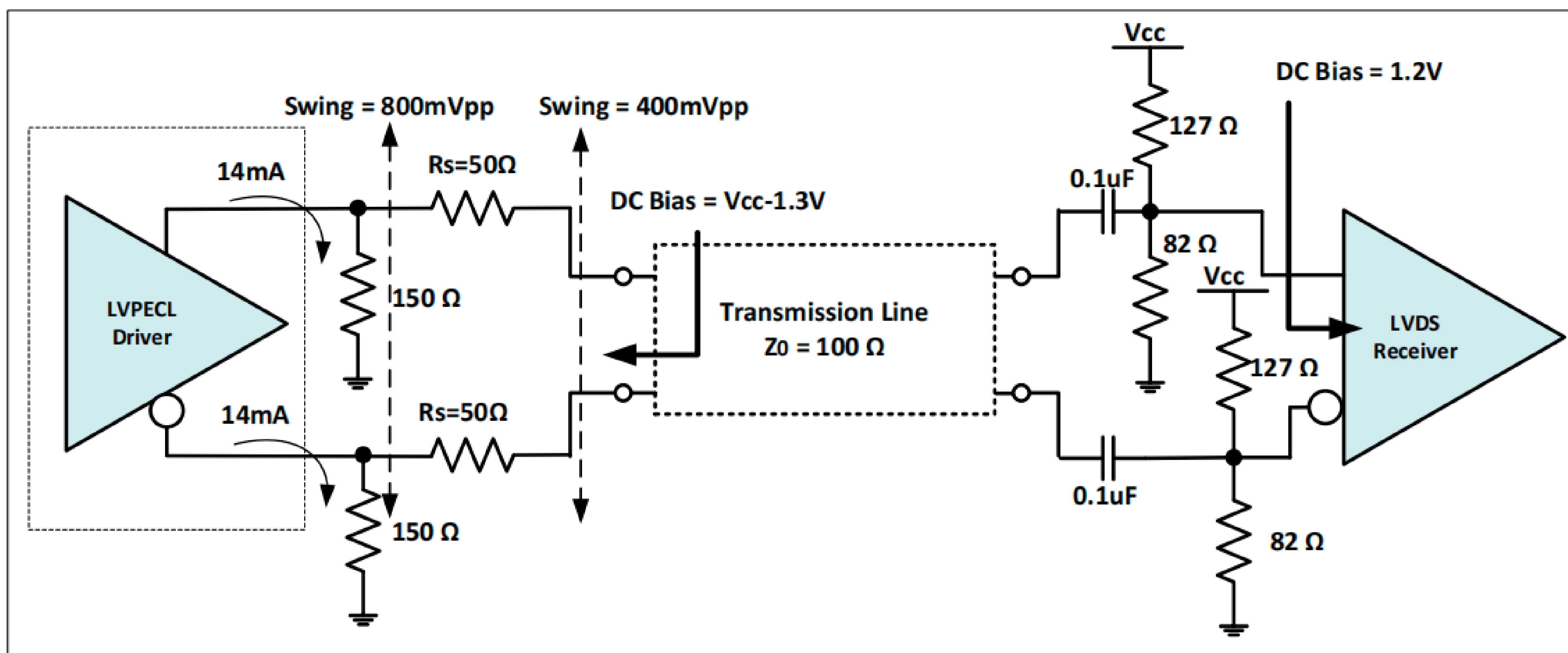
Similar principal is used for LVPECL-to-LVDS to change the common mode voltage. Here we have option of reducing the swing voltage (Vpp) according to the capability of receiver.



Common mode calculation for LVDS

$$V_{cm} = \frac{10k}{(10k + 16k)} \times 3.3V = 1.26V$$

Another way of terminating and providing common mode at LVDS receiver is shown using block diagram below.



Common mode calculation for LVDS receiver -

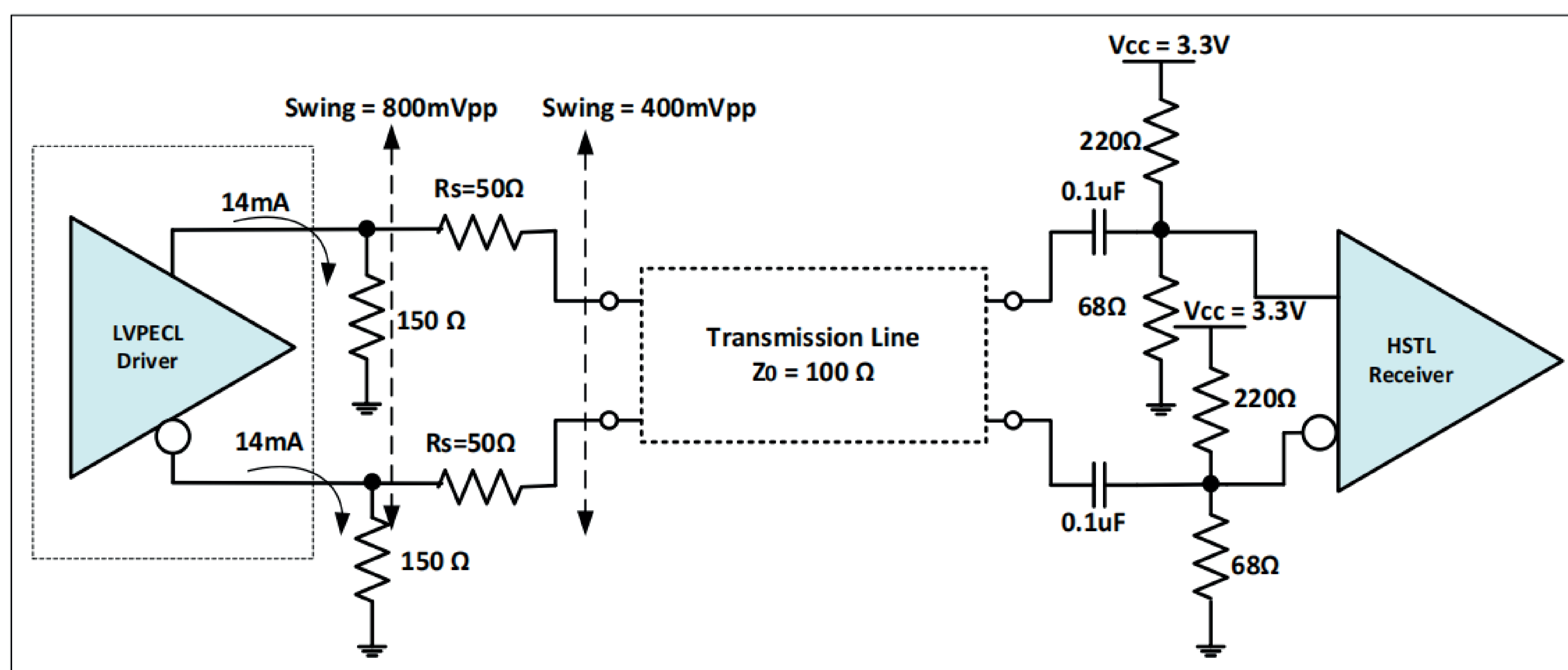
$$V_{cm} = \frac{82}{(82 + 127)} \times 3.3V = 1.29V$$

Thévenin Termination Calculation for each line = Rth

$$R_{th} = \frac{82 \times 127}{(82 + 127)} = 50\Omega$$

#### 4. LVPECL to HSTL Conversion

Similar principal is used for LVPECL-to-HSTL to change the common mode voltage to 0.75V. Here the option of reducing the swing voltage ( $V_{pp} = 400mV$ ) according HSTL standard is given using  $R_s$  resistors.



Common mode calculation for HSTL receiver -

$$V_{cm} = \frac{68}{(68 + 220)} \times 3.3V = 0.75V$$

Thévenin Termination Calculation for each

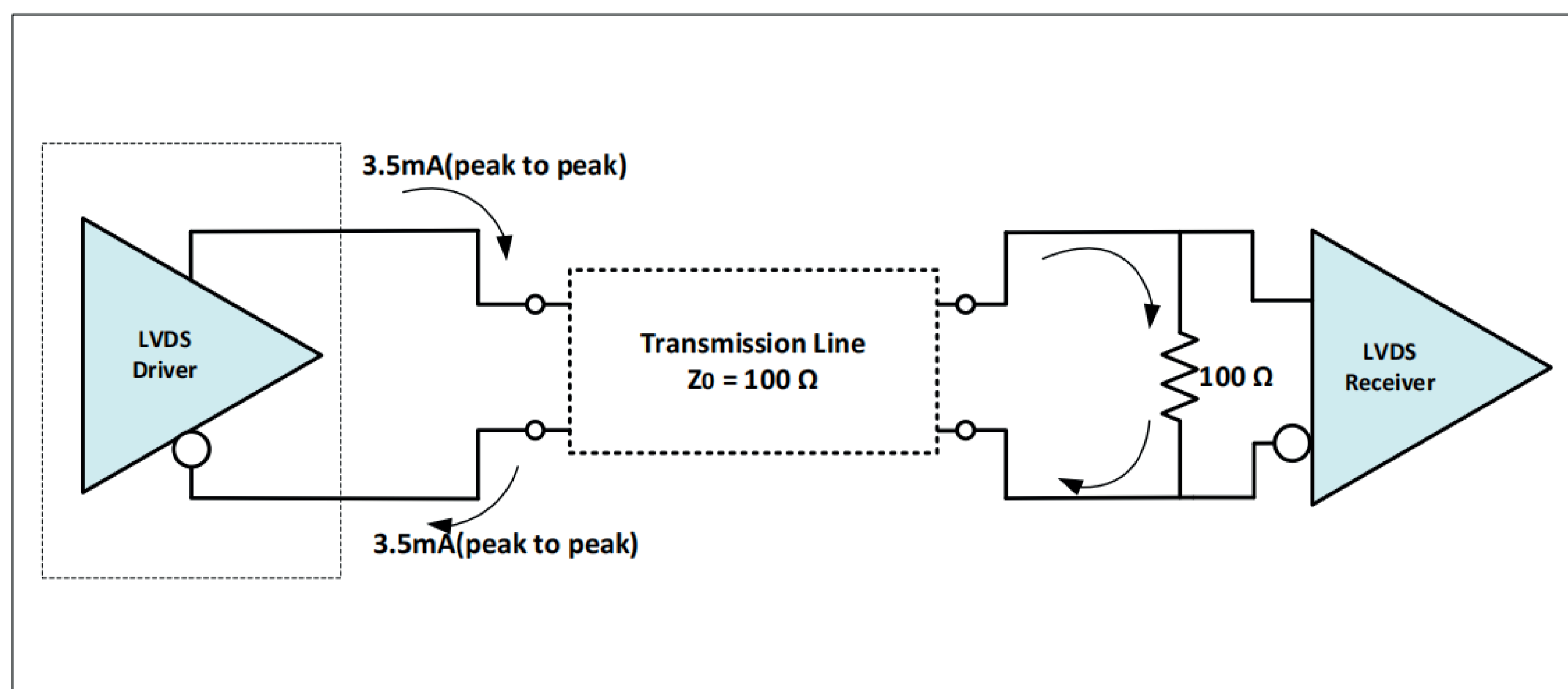
$$R_{th} = \frac{68 \times 220}{(68 + 220)} = 50 \Omega$$

Calculation to change the swing at receiver

$$V_{pp}(\text{receiver}) = \frac{100}{(100 + 2 \times 50)} \times 800 = 400 \text{mV}$$

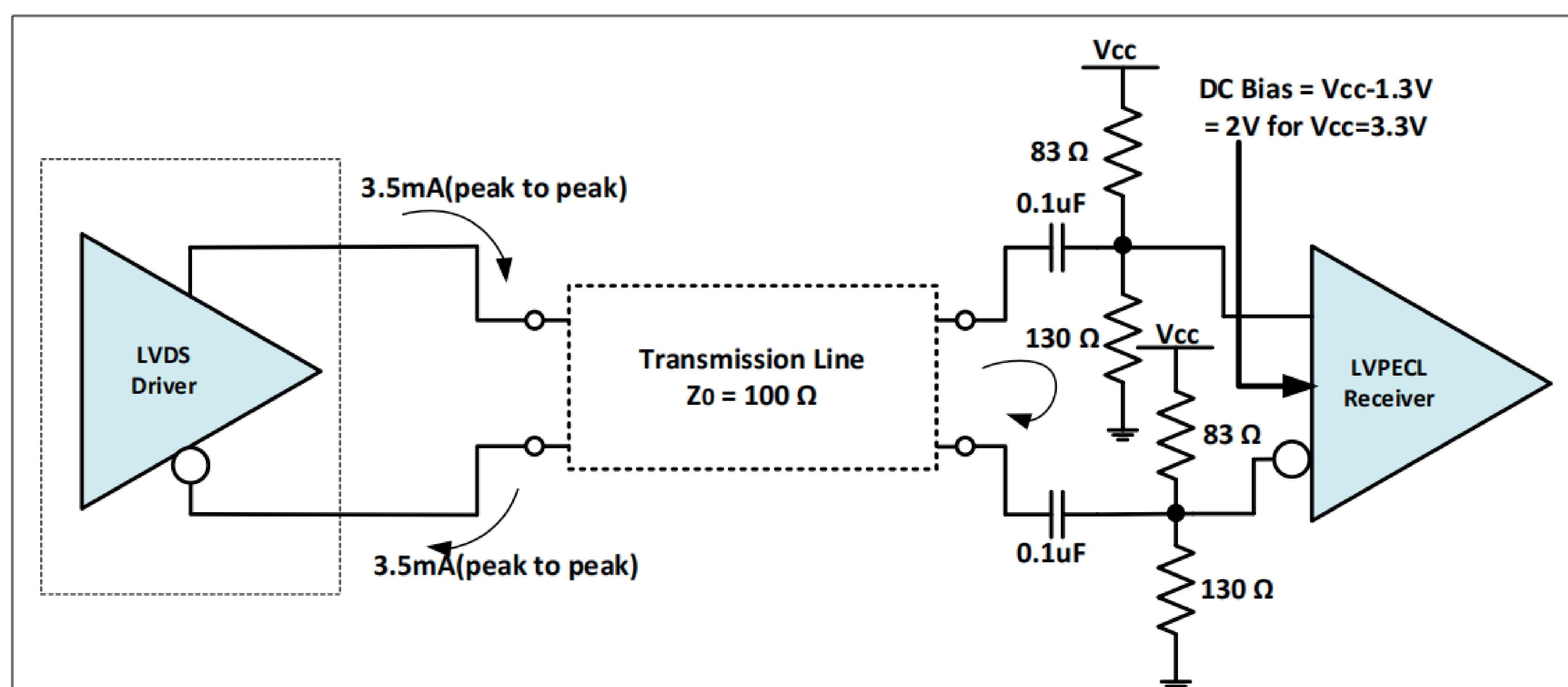
### 5. LVDS to LVDS Conversion

LVDS is another type of differential signalling and it is again a current source signalling. Receiver senses only voltage so, it is necessary to use termination resistance of suitable value to convert the current to the voltage. As Low Voltage Differential Signal (LVDS) has lower swing and speed than its alternatives like LVPECL, CML, VML, it consumes relatively low power. The current sourced by LVDS driver is 3.5-4mA which converts to 350-400mVpp swing when the current passes through termination resistance of 100Ω. A 100Ω parallel termination between positive and negative line should be there at receiver. It acts as current to voltage converter as well as load resistor. LVDS receivers of Xilinx FPGA (either LVDS\_18 or LVDS\_25) provide internal termination resistor, so 100Ω external termination is not needed. External termination of 100Ω is required for LVDS\_33 and LVDS\_15. Coupling capacitors have not been added here as both source and receiver have same common mode as both are LVDS.

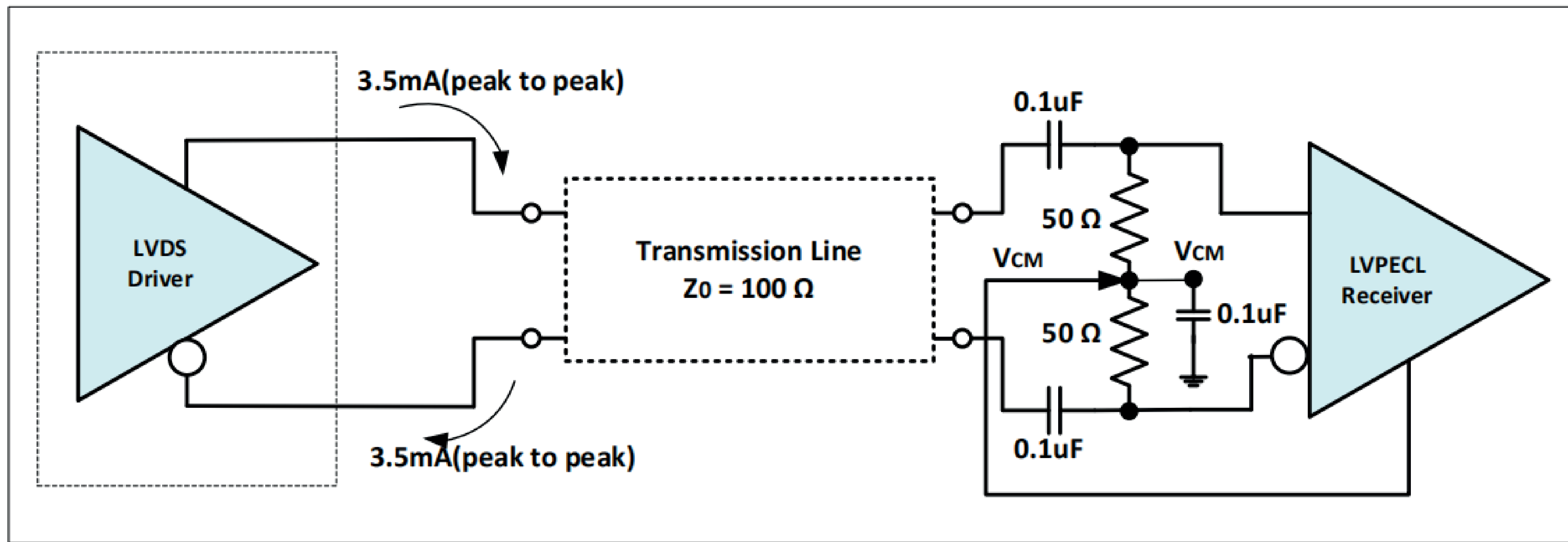


### 6. LVDS to LVPECL Conversion

Here is differences of common mode of LVDS (1.2V) to common mode of LVPECL (2V for 3.3 VCC) and swing (400mV of LVDS to 800mVpp max of LVPECL). As LVPECL's minimum acceptable swing is 310mV, it accepts signals of 400mVpp. Block diagram for LVDS-to-LVPECL conversion is shown below.

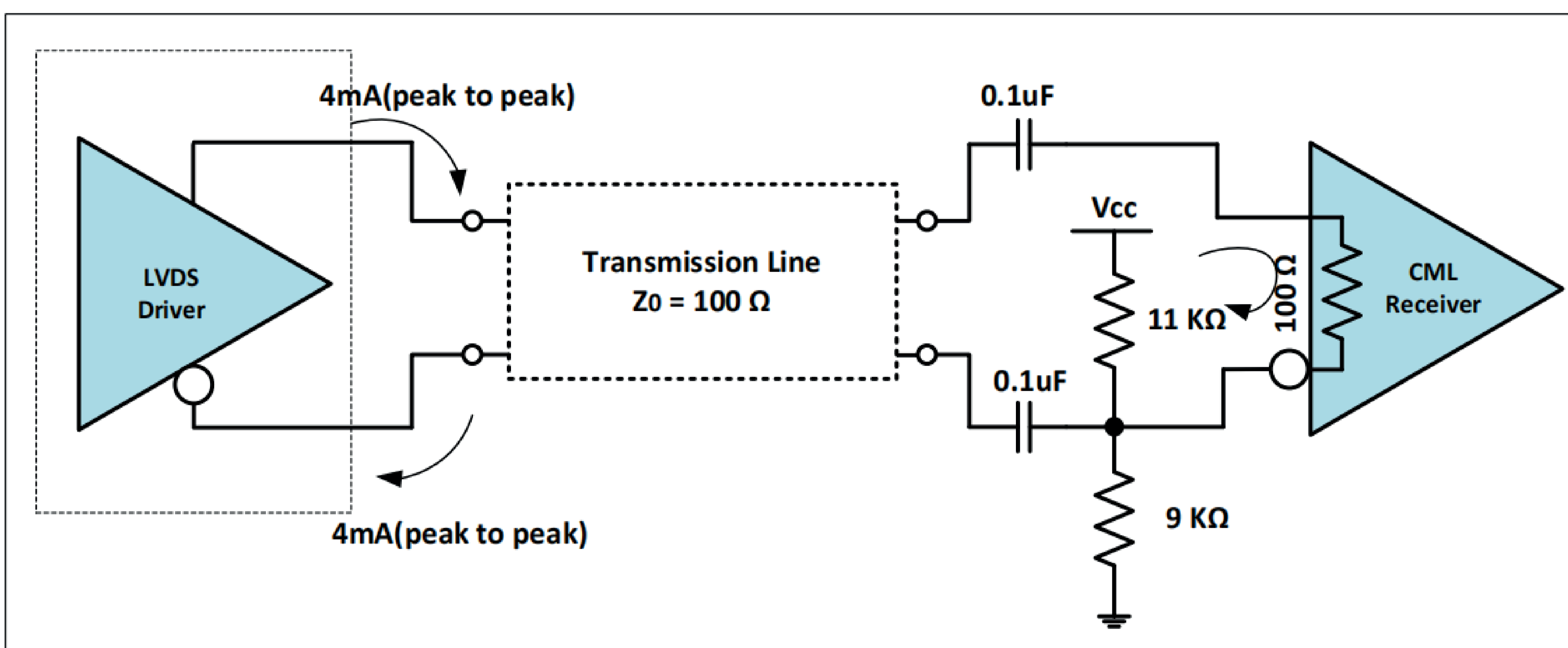


Whenever, input common mode voltage is provided by the LVPECL receiver itself, resistor divider circuit is not used. It is shown below.



### 7. LVDS to CML Conversion

LVDS-to-CML uses same basic method to change the common-mode. Resistor divider circuit of 10kΩ resistors, provide the common mode voltage for the receiver circuit. 100Ω resistor provides load termination as well as it converts the current into its equivalent voltage to 400mVpp. 400mVpp comes under CML acceptable range of voltage swing. For Xilinx FPGA,

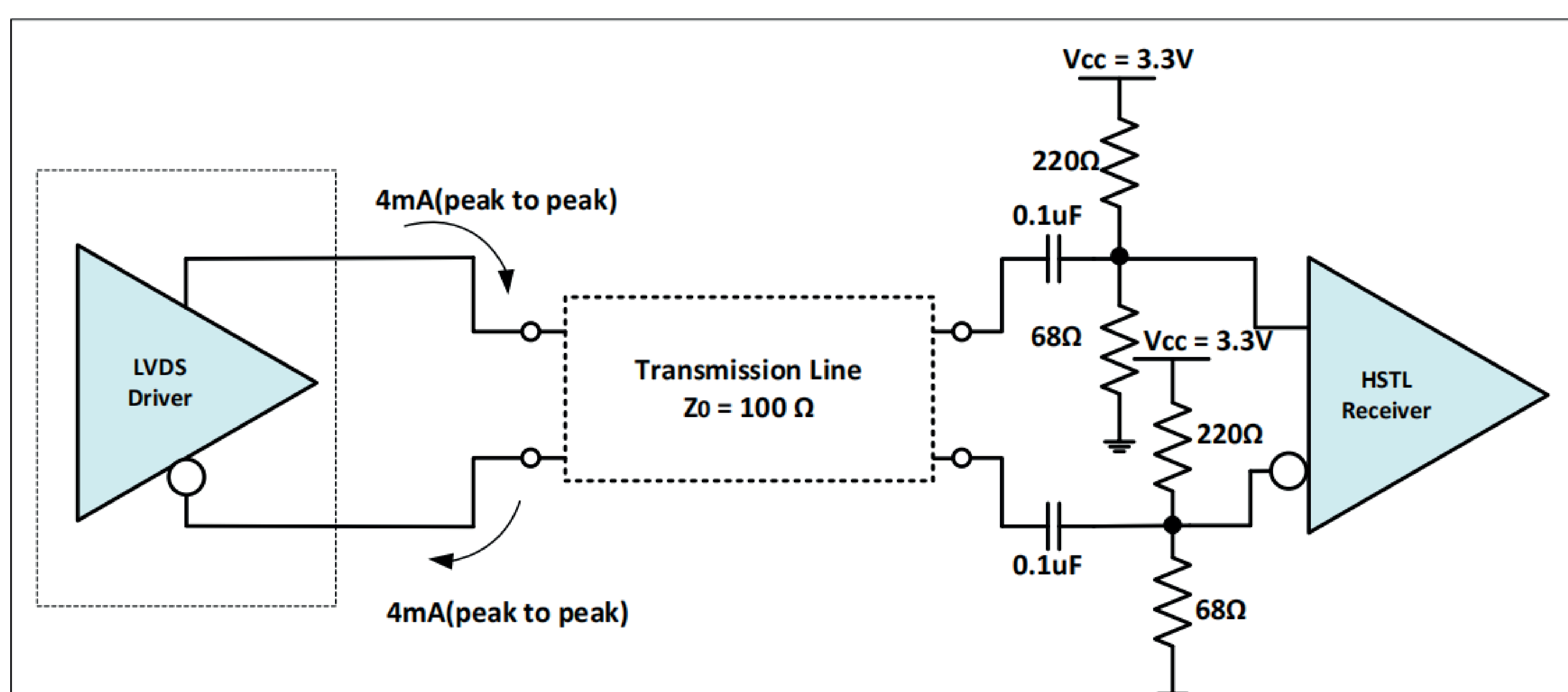


Common mode calculation for LVDS receiver -

$$V_{cm} = \frac{9k}{(9k + 11k)} \times 3.3V = 1.5V$$

### 8. LVDS to HSTL Conversion

LVDS-to-CML conversion uses two resistors 220Ω and 68Ω in parallel configuration to provide common mode of 0.75V. 400mVpp swing is under acceptable range of HSTL receiver.





Common mode calculation for HSTL receiver -

$$V_{cm} = \frac{68}{(68 + 220)} \times 3.3V = 0.75V$$

Thévenin Termination Calculation for each line = Rth

$$R_{th} = \frac{68 \times 220}{(68 + 220)} = 50\Omega$$

Calculation to change the swing at receiver

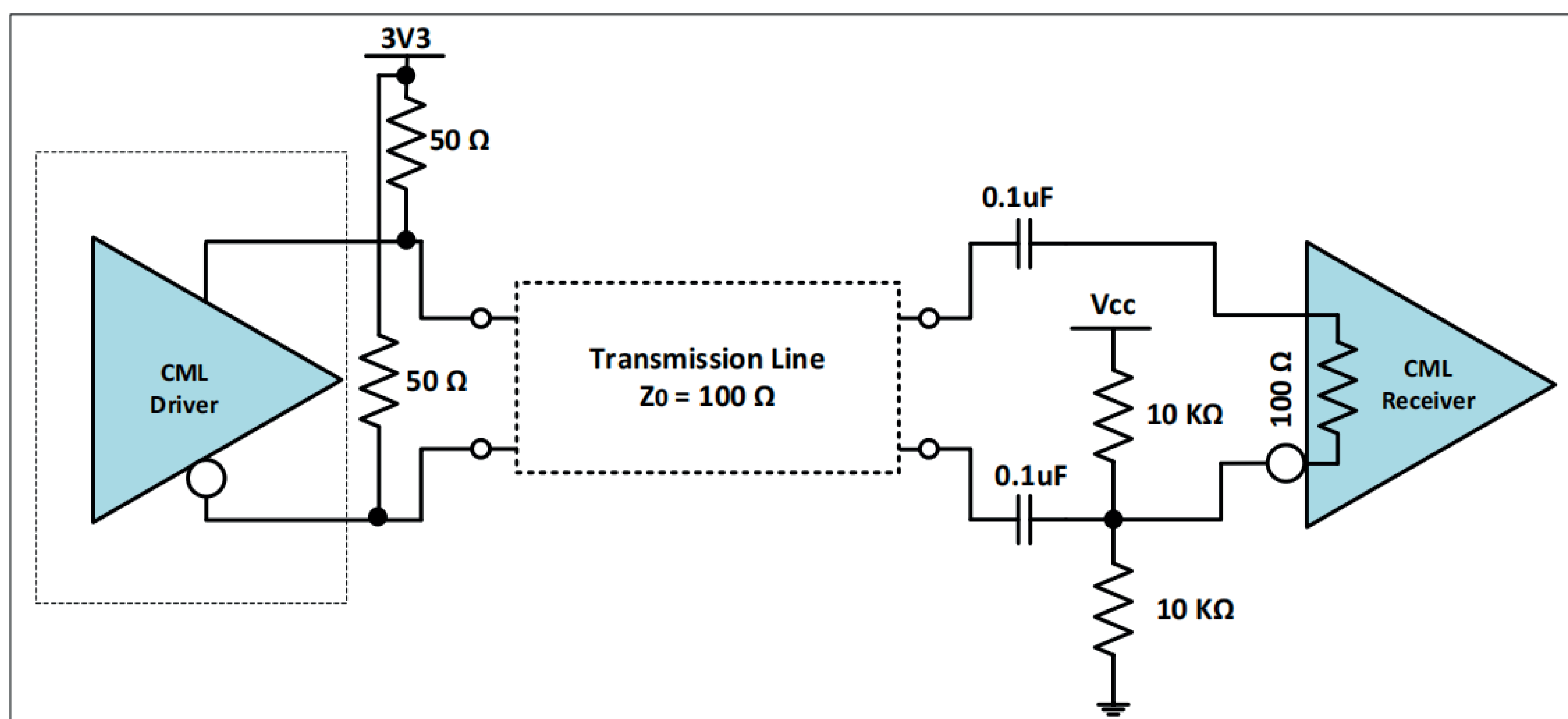
$$V_{pp}(\text{receiver}) = 4\text{mA} \times 100\Omega = 400\text{mV}$$

### 9. CML to CML

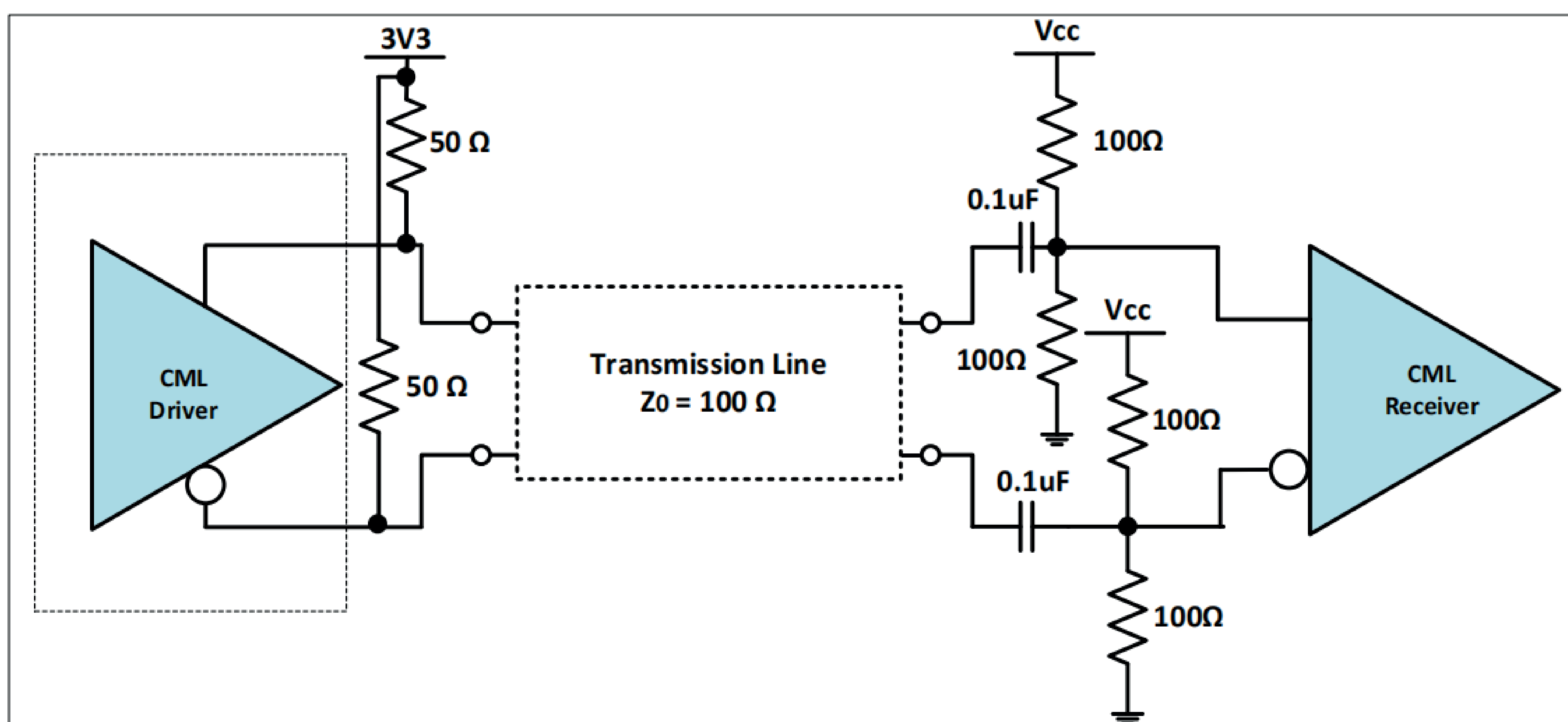
CML (Current Mode Logic) uses open-source NMOS transistors, it cannot rise the signal to state '1' similar to open-drain system. That's why it needs 50Ω pull-up resistors to Vcc to make the signal '1'. 50Ω is chosen to avoid reflection in the transmission lines.

This 50Ω pull up termination is not externally required for Xilinx FPGA GTX CML outputs as there is internal configurable pull-ups to MGTAVTT available.

CML-to-CML conversion has source and receiver terminations. 100Ω termination is required at receiver end. Two register each of 10kΩ is required to get common mode close to 1.5V.

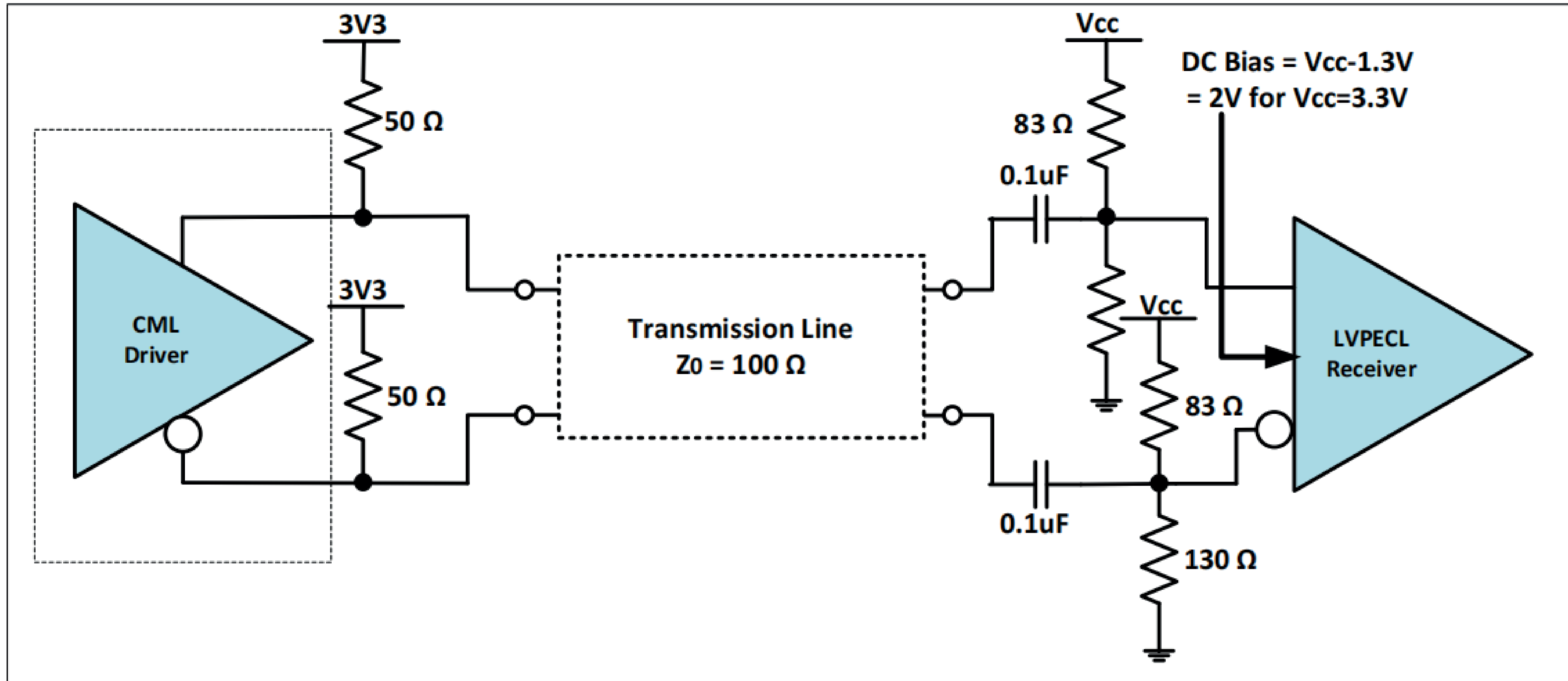


If internal termination is not available at receiver end, it can be terminated as below. Two 100Ω resistors provide common mode as well as termination of effective 50Ω load termination on each line.



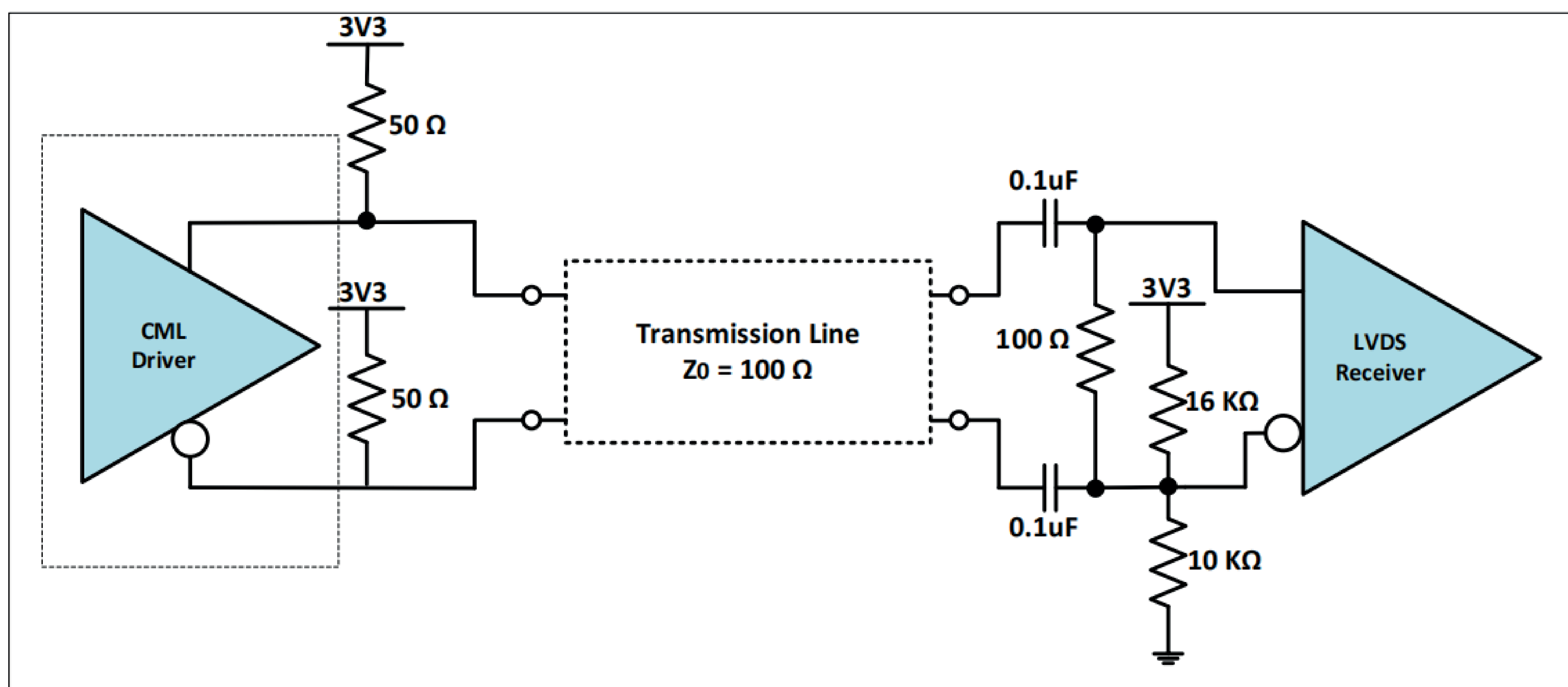
### 10. CML to LVPECL Conversion

CML-to-LVPECL conversion has same strategy of CML source termination, AC coupling, and common mode cum receiver termination using Thevenin architecture. Register divider circuit using  $130\Omega$  and  $83\Omega$  make Thevenin resistance of  $50\Omega$  and common mode of  $V_{cc}-2V$ .  $V_{pp}$  of CML is  $800mV$  which is under acceptable range of LVPECL receiver's  $V_{pp}$  range.



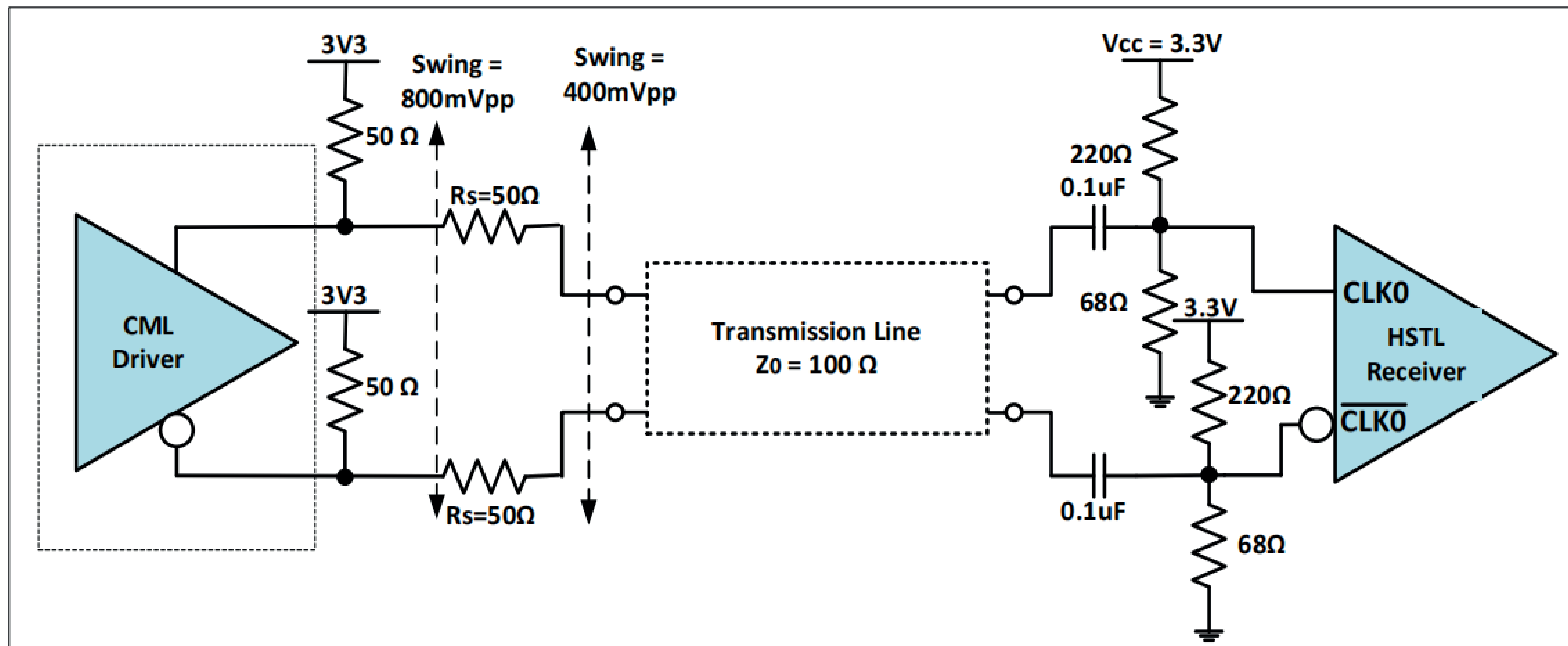
### 11. CML to LVDS Conversion

CML-to-LVDS conversion has same strategy of CML source termination, AC coupling, and common mode cum receiver termination using Thevenin architecture.  $100\Omega$  termination is used to provide load termination and  $10k\Omega$  resistor divider circuit used for providing common mode of  $1.2V$  for LVDS receiver.



## 12. CML to HSTL Conversion

CML-to-HSTL conversion has same strategy of CML source termination, AC coupling, and common mode cum receiver termination using Thevenin architecture. The architecture uses two resistors 220Ω and 68Ω in parallel configuration to provide common mode of 0.75V. Option for reducing source Vpp to receiver voltage swing of 400mV is given using two Rs 50Ω resistors.



Common mode calculation for HSTL receiver -

$$V_{cm} = \frac{68}{(68 + 220)} \times 3.3V = 0.75V$$

Thevenin Termination Calculation for each line = Rth

$$R_{th} = \frac{68 \times 220}{(68 + 220)} = 50\Omega$$

Calculation to change the swing at receiver

$$V_{pp}(\text{receiver}) = \frac{100}{(100 + 2 \times 50)} \times 800 = 400mV$$

# Thank You!

Does anyone have any questions?

Contact Us



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