logic fruit Technologies

Whitepaper

PCIe Gen6

Retimer Equalization

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Equalization

Equalization is the process of compensating the distortion introduced by the channel. After passing through a band-limited channel, the high frequency components of the signal are heavily attenuated which distorts the signal and spreads it into subsequent symbol periods.

Implementaion of Equalization is prefered on Tx side where signal is free from noise.

While equalization was implemented on the Tx side with a 3-tap FIR filter in PCIe Gen 3 through 5, it is implemented with a 4-tap FIR filter in PCIe Gen 6 as shown in Figure 1 & 2. Four consecutive pulses are multiplied with their respective coefficients and added to generate the filter output.

The coefficients C_{-2}, C_{-1}, C_0, and C_{+1} are called 2nd precursor, precursor, cursor and postcursor.

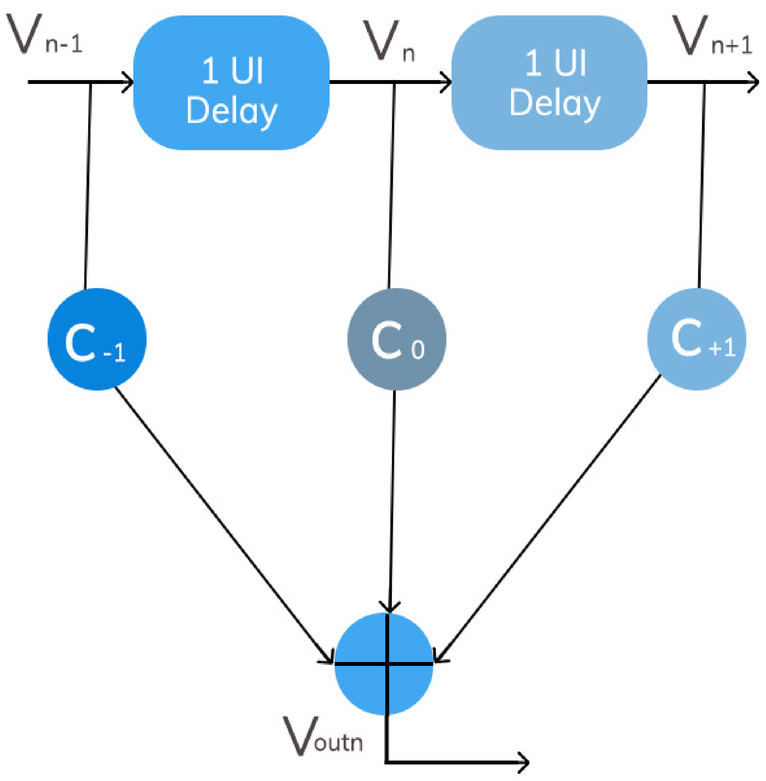


Figure 1 : FIR Filter Gen3/4/5

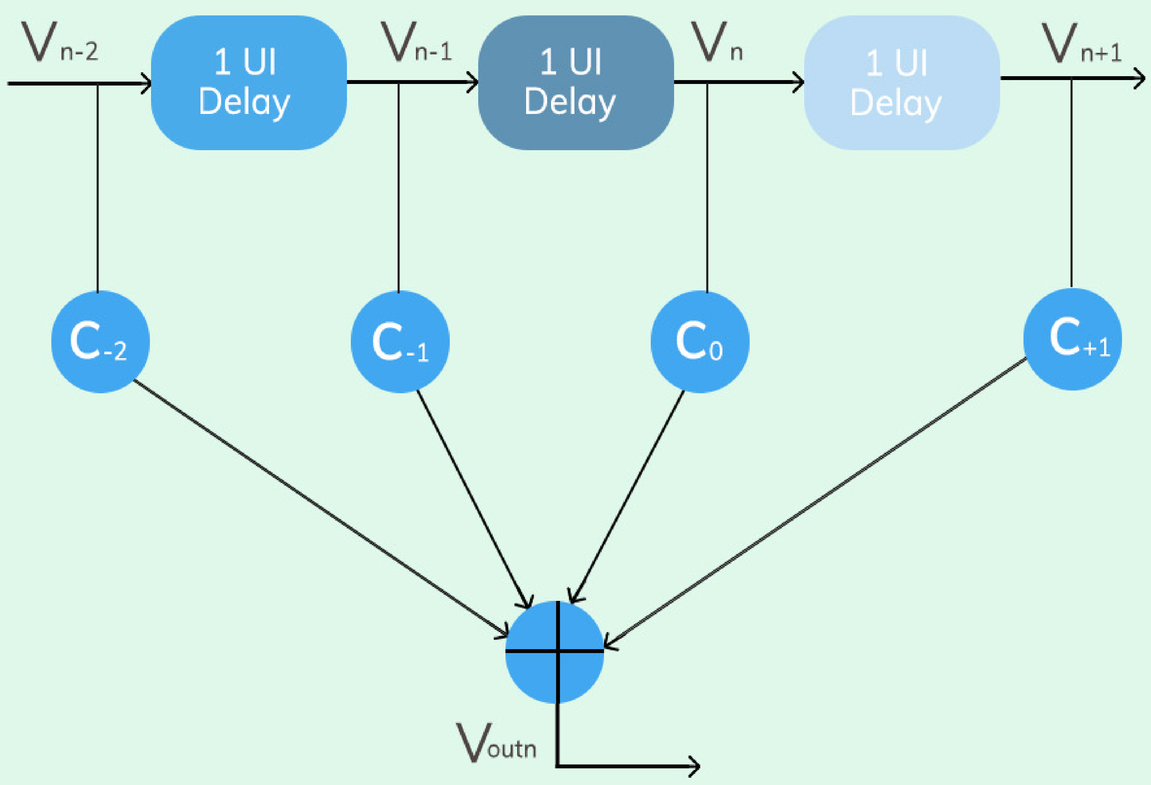


Figure 2 : FIR Filter Gen6

Gen3/4/5

While equalization is requested by a device, then state machine tranction happens by sending/reciving TS1 and TS2 order sets.The equalization procedure consists of up to four Phases, as described below. The Phase information is transmitted using the Equalization Control (EC) field (Symbol 6, Bit 1:0) in the TS1 Ordered Sets.

Gen6

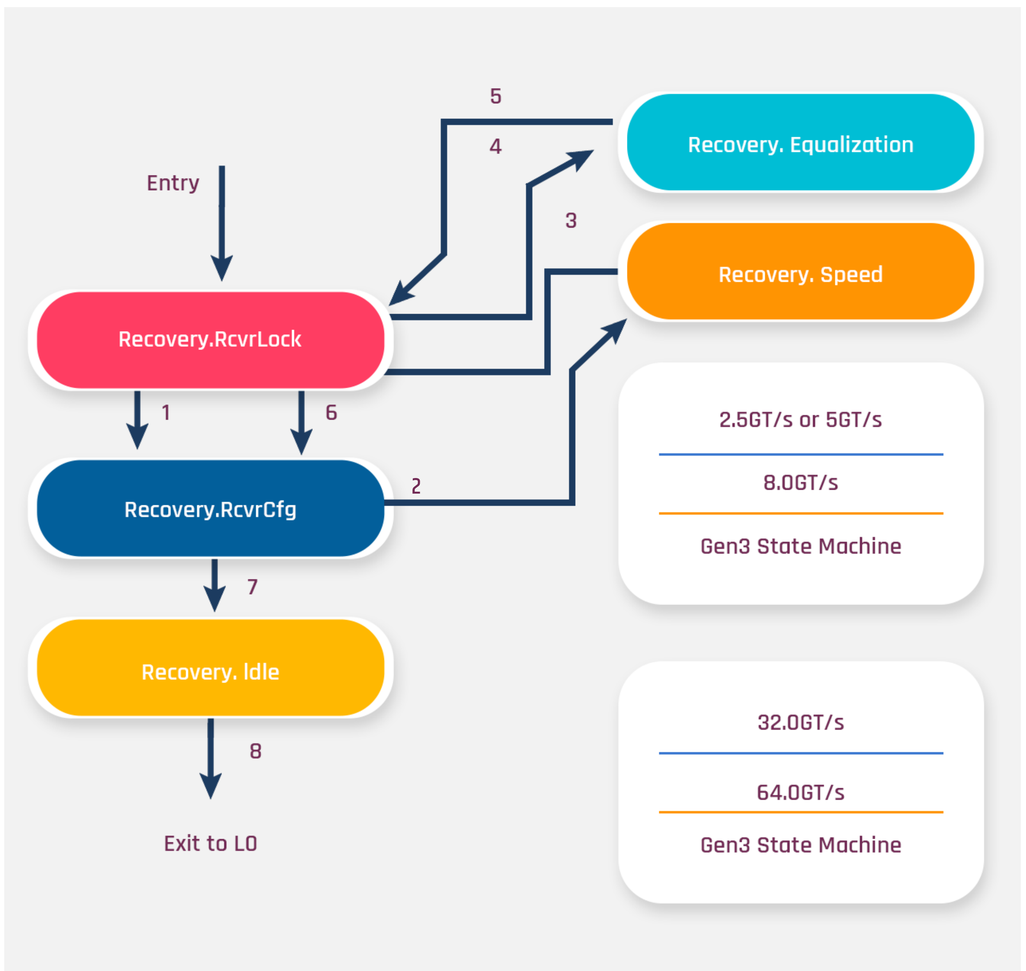
PCIe gen6 introduces a new ordered set TS0 with functionality similar to that of TS1, and changes the definition of TS1 and TS2 ordered sets to incorporate replication of data. TS0 has alternate bits set to 0, to enable its representation using only two voltage levels (0 and 3) in PAM4, which is essentially equivalent to NRZ. This allows for easy detection in the initial stages of equalization when the link is not fully trained.

Current Data rate/Port	Phase0/ Phase1	Phase2	Phase3
8/16/32 GT/s; DP	TS1	TS1	TS1
8/16/32 GT/s; UP	TS1	TS1	TS1
64 ; DP	TS0	TS1	TS1
64 ; UP	TS0	TS0	TS1

Table 1: Use of TS0 vs TS1 in diff phases

Phase 0: The Upstream port(UP) sends TS0 with EC=00b, and preset values it received in Recovery.RcvrCfg. Downstream Port (DP) directly starts with Phase 1.

Next phase for the UP is Phase 1 if all the configured Lanes receive two consecutive TS0/TS1 Ordered Sets with EC = 01b or if all the configured Lanes receive two consecutive TS0 Ordered Sets with EC = 01b and Retimer Equalization Extend(REE) bit set to 0b.



Phase 1: The DP transmit TS0 with EC = 01b, and preset field set to the preset value it is currently using. The UP, receives these TS0 ordered sets and transitions to Phase 1, where it also transmits TS0 with EC = 01b, and preset field set to the current preset value. Both ports exchange LF and FS values.

Phase 2: The DP transmits TS1 with EC=10b. The UP follows after receiving two consecutive TS1 with EC = 10b. In this phase the UP helps the DP fine tune its transmitter setting along with its own receiver setting until a BER of less than 10-6 is achieved. The UP requests the DP to either apply presets or coefficients by indicating it in the use_preset field in TS0.

The DP after receiving two consecutive TS0 ordered sets with the same request, chooses to either accept or reject the requested settings, and starts sending TS1 with the requested settings and the reject_coefficient bit set to 0 or 1 accrordingly.

In case the requests are accepted, the UP evaluates the settings and requests new settings if required. This continues until the required BER is achieved, after which the UP makes the transition to Phase 3 after sending TS0 with EC=11b.

Phase 3: The DP also makes the transition to Phase 3 after receiving two consecutive TS1 with EC = 11b. In this phase the DP helps the UP fine tune its transmitter setting along with its own receiver setting until a BER of less than 10-6 is achieved after following a method similar to Phase 2. The DP sends TS1 with EC = 00b to indicate that it is satisfied with the BER and thus the end of equalization procedure.

Retimer

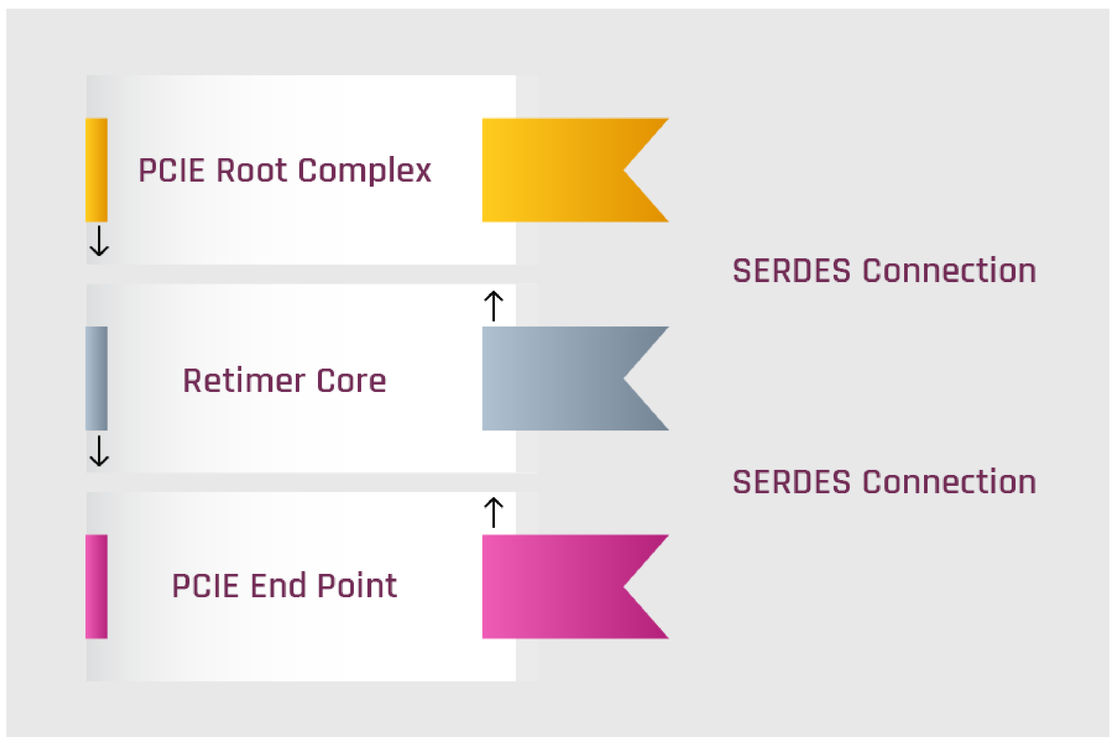
Retimer equalization is used for maintaining signal integrity and ensuring reliable data communication in high-speed serial data links. It helps overcome the challenges posed by long or lossy channels and enhances interoperability.

Retimer equalization involves the use of retimer or signal regenerator devices that receive incoming signals, clean them up, and then retransmit them. This process includes re-clocking the data and reshaping the signal to reduce jitter and noise. The retimer essentially takes in a potentially degraded signal and outputs a cleaner, more robust version.

A maximum of two Retimers are permitted between an Upstream and a Downstream Port. Retimers have two Pseudo Ports, one facing Upstream, and the other facing Downstream. The Transmitter of each Pseudo Port must derive its clock from a 100 MHz reference clock.

The Pseudo Port orientation (Upstream or Downstream) is determined dynamically, while the Link partners are in Configuration. Both crosslink and regular Links are supported.

In most operations Retimers simply forward received Ordered Sets, DLLPs, TLPs, Logical Idle, and Electrical Idle. Retimers are completely transparent to the Data Link Layer and Transaction Layer.



Retimer Equalization Procedure

Retimer has two Pseudo Ports, which dynamically determine their Downstream/ Upstream orientation dynamically. Retimer has an Upstream Path and a Downstream Path. Both Pseudo Ports must always operate at the same data rate, when in Forwarding mode. Thus, each Path will also be at the same data rate. The behavior of the Retimer in each high level operating mode is:

- ***Forwarding mode:-*** Symbols, Electrical Idle, and exit from Electrical Idle; are forwarded on each Upstream and Downstream Path.

☞ ***Execution mode:-*** The Upstream Pseudo Port acts as an Upstream Port of a Component. The Downstream Pseudo Port acts as a Downstream Port of a Component. This mode is used in the following cases:

- Phase 2 and Phase 3 of the Link equalization procedure.
- Optionally Follower Loopback.

Retimer Equalization Phases:

Downstream Ports directly starts with Phase 1 in equalization.

UPP phase 0: During this phase, the UPP sends TS0/TS1s with EC = 00b while using the Transmitter Preset values that were delivered in the EQ TS2s before entering this state. The equalization information fields in the TS0/TS1s being sent must show the preset value and also the Pre-cursor, Cursor, and Post-cursor coefficient fields that correspond to that preset.When all configured Lanes receive two consecutive TS0/TS1s with EC = 01b, and Retimer Equalization Extend bit set to 0b then the next phase is Phase 1.

If the data rate of operation is 64.0 GT/s or above, the Retimer Equalization Extend bit of the transmitted TS0 Ordered Sets is set to 1b when the Downstream Pseudo Port state is Phase 1 and is transmitting TS0 Ordered Sets with the EC = 00b otherwise it is set to 0b. This helps in synchronization if multiple retimers are used.

The LF and FS values received in the two consecutive TS0/TS1 Ordered Sets must be stored for use during Phase 2 to adjust the Downstream Port's Transmitter coefficients.

Note: In Phase 1, TS0s with EC = 00b are sent for long time only if REE bit is 1b in the received ordered sets.

DPP phase 1: The DPP sends TS0/TS1s with EC = 01b while using the Preset values from the Lane Equalization Control register.The FS (Full Swing), LF (Low Frequency), Pre-cursor, Cursor and Post-cursor Coefficient fields that correspond to the Transmitter Preset field are also taken from the Lane Equalization Control register. Downstream can wait upto 500 ns before evaluating the received ordered sets. The next phase is Phase 2 if all configured Lanes receive two consecutive TS1 Ordered Sets with EC = 01b and the Downstream Pseudo Port wants to execute Phase 2 and Phase 3.

If the data rate of operation is 64.0 GT/s or above, the Retimer Equalization Extend bit of the transmitted TS0 Ordered Sets is set to 1b when the Upstream Pseudo Port state is Phase 0, and it is set to 0b when the Upstream Pseudo Port state is Phase 1. This helps in synchronization if multiple retimers are used.

The LF and FS values received in the two consecutive TS1 Ordered Sets with EC = 01b must be stored for use during Phase 3, to adjust the Upstream Port's Transmitter coefficients.

UPP phase 1: The Phase 1 of UPP is called Phase 1 Active in Retimer EQZ, but there are no differences from normal equalization.

During this phase, the UPP sends TS1s with EC = 01b while using the Transmitter settings that were determined in Phase 0. These TS1s contain the FS, LF, and Post-cursor Coefficient values which are currently being used.

Next phase is Phase 2 if all configured Lanes receive two consecutive TS0/TS1 Ordered Sets with EC = 10b.

DPP phase 2: Transmitter sends TS1 Ordered Sets with EC = 10b and the coefficient settings, set on each Lane independently.
If two consecutive TS1s are received with EC = 10b (Upstream Port has entered Phase 2), and if the values requested are legal and supported, then change the Transmitter settings to use them within 500ns of the end of the second TS1 requesting them.

If the requested preset or coefficients are illegal or not supported, don't change the Transmitter settings but reflect the received values in the TS1s being sent and set the Reject Coefficient Values bit to 1b.

If the two consecutive TS1s aren't seen, keep the current Transmitter preset and coefficient values.
If the data rate of operation is 16.0 GT/s or above, the Retimer Equalization Extend bit of the transmitted TS1 Ordered Sets is set to 1b when the Upstream Pseudo Port state is Phase 2 Active, and it is set to 0b when the Upstream Pseudo Port state is Phase 2 Passive.

Next phase is Phase 3 Active if all configured Lanes receive two consecutive TS1 Ordered Sets with EC = 11b.

Note: Retimer Equalization Extend bit is reserved at Gen3 data rate.

UPP phase 2: Phase 2 Equalization for UPP is done in two sub Phases, Phase 2 Active and Phase 2 Passive.

UPP phase 2 Active: The UPP sends TS1s with EC = 10b. The UPP can request a new preset by putting a legal value in the Transmitter Preset field of the TS1s being sent and setting the Use Preset bit to 1b to tell the Downstream Port to begin using it or request new coefficients by putting legal values in those fields and clearing the Use Preset bit to 0b so the Downstream Port will load them instead of the preset field.

The Upstream Port must wait long enough to ensure the Downstream Transmitter has had a chance to implement the requested changes, (500ns plus the round-trip delay for the logic), and evaluate the incoming TS1s.

The Retimer Equalization Extend bit of transmitted TS1 Ordered Sets is set to 0b. Next phase is Phase 2 Passive if all configured Lanes are operating at their optimal settings and all configured Lanes receive two consecutive TS1 Ordered Sets with the Retimer Equalization Extend bit set to 0b.

UPP phase 2 Passive: Transmitter sends TS1 Ordered Sets with EC = 10b, Retimer Equalization Extend = 0b, and the Transmitter Preset field and the Coefficients fields must not be changed from the final value transmitted in Phase 2 Active.
If the data rate of operation is 8.0 GT/s, the next state is Phase 3 when the Downstream Pseudo Port has completed Phase 3 Active.

If the data rate of operation is 16.0 GT/s or above, the next state is Phase 3 when the Downstream Pseudo Port has started Phase 3 Active.

DPP phase 3: Phase 3 Equalization for DPP is done in two sub Phases, Phase 3 Active and Phase 3 Passive.

UPP phase 3 Active: The DPP sends TS1s with EC = 11b and begins the process of evaluating Upstream Tx settings independently for each Lane.

In the transmitted TS1s, the DPP can either request a new preset by setting the Use Preset bit to 1b and Transmitter Preset field to the desired value, or it can request new coefficients by clearing the Use Preset bit to 0b and setting the Pre-cursor, Cursor, and Post-Cursor Coefficient fields to the desired values.

The DPP must wait long enough to ensure the Upstream Transmitter has had a chance to implement the requested changes, (500ns plus the round-trip delay for the logic), then obtain Block Alignment and evaluate the incoming TS1s.

The Retimer Equalization Extend bit of transmitted TS1 Ordered Sets is set to 0b.

The next phase is Phase 3 Passive if all configured Lanes are operating at their optimal settings and all configured Lanes receive two consecutive TS1 Ordered Sets with the Retimer Equalization Extend bit set to 0b.

UPP phase 3 Passive: Transmitter sends TS1 Ordered Sets with EC = 11b, Retimer Equalization Extend = 0b, and the Transmitter Preset field and the Coefficients fields must not be changed from the final value transmitted in Phase 3 Active.

The transmitter switches to Forwarding mode when the Upstream Pseudo Port exits Phase 3.

UPP phase 3: The UPP sends TS1s with EC = 11b and responds to the requested Transmitter values from the Downstream Port. If two consecutive TS1s aren’t seen, keep the current Transmitter preset and coefficient values.

If the values requested are legal and supported, then change the Tx settings to use them within 500ns of the end of the second TS1 requesting them.

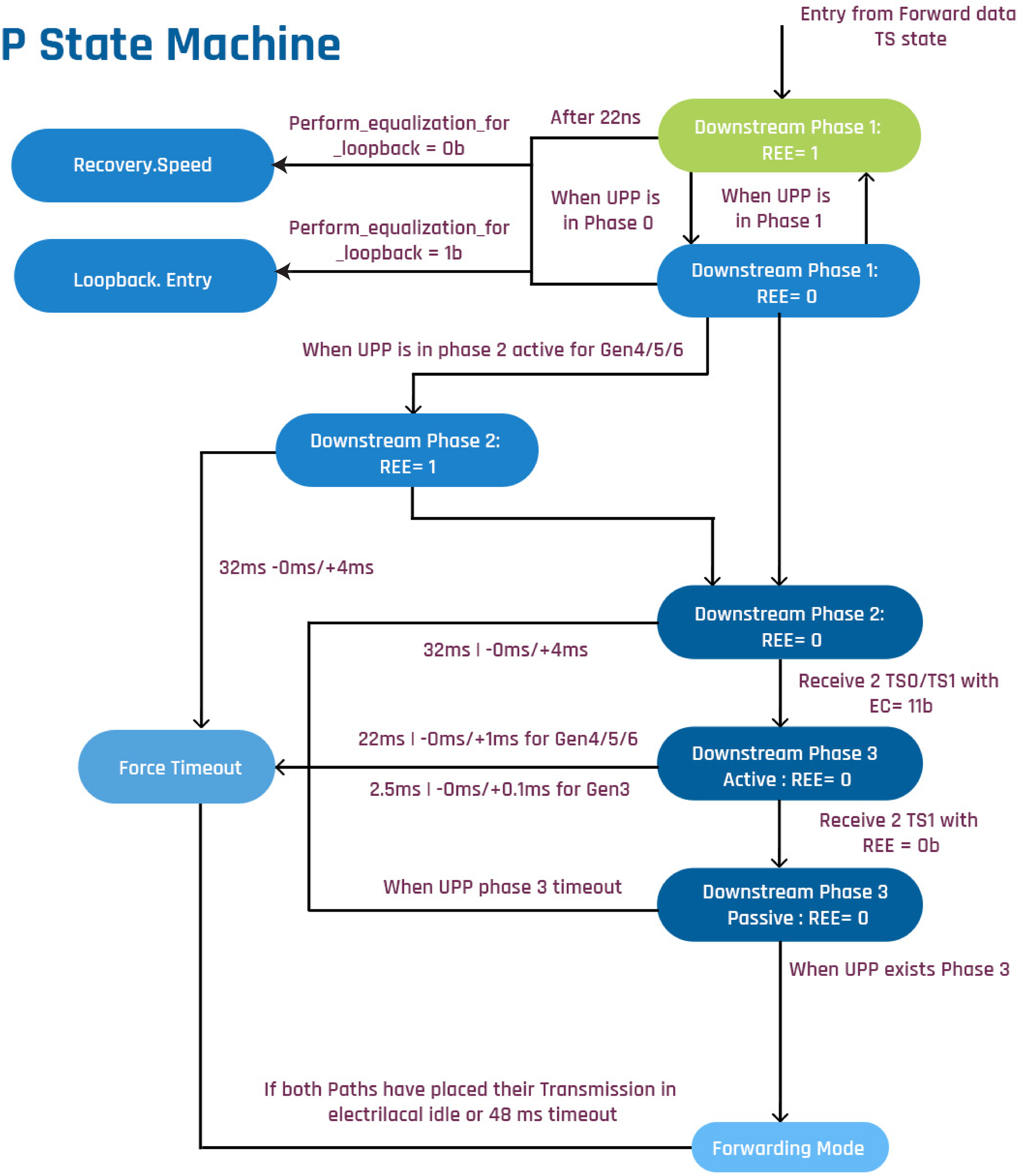
If the requested preset or coefficients are illegal or not supported, don’t change the Transmitter settings but reflect the received values in the TS1s being sent and set the Reject Coefficient Values bit to 1b.

If the data rate of operation is 16.0 GT/s or above, the Retimer Equalization Extend bit of the transmitted TS1 Ordered Sets is set to 1b when the Downstream Pseudo Port state is Phase 3 Active, and it is set to 0b when the Downstream Pseudo Port state is Phase 3 Passive.

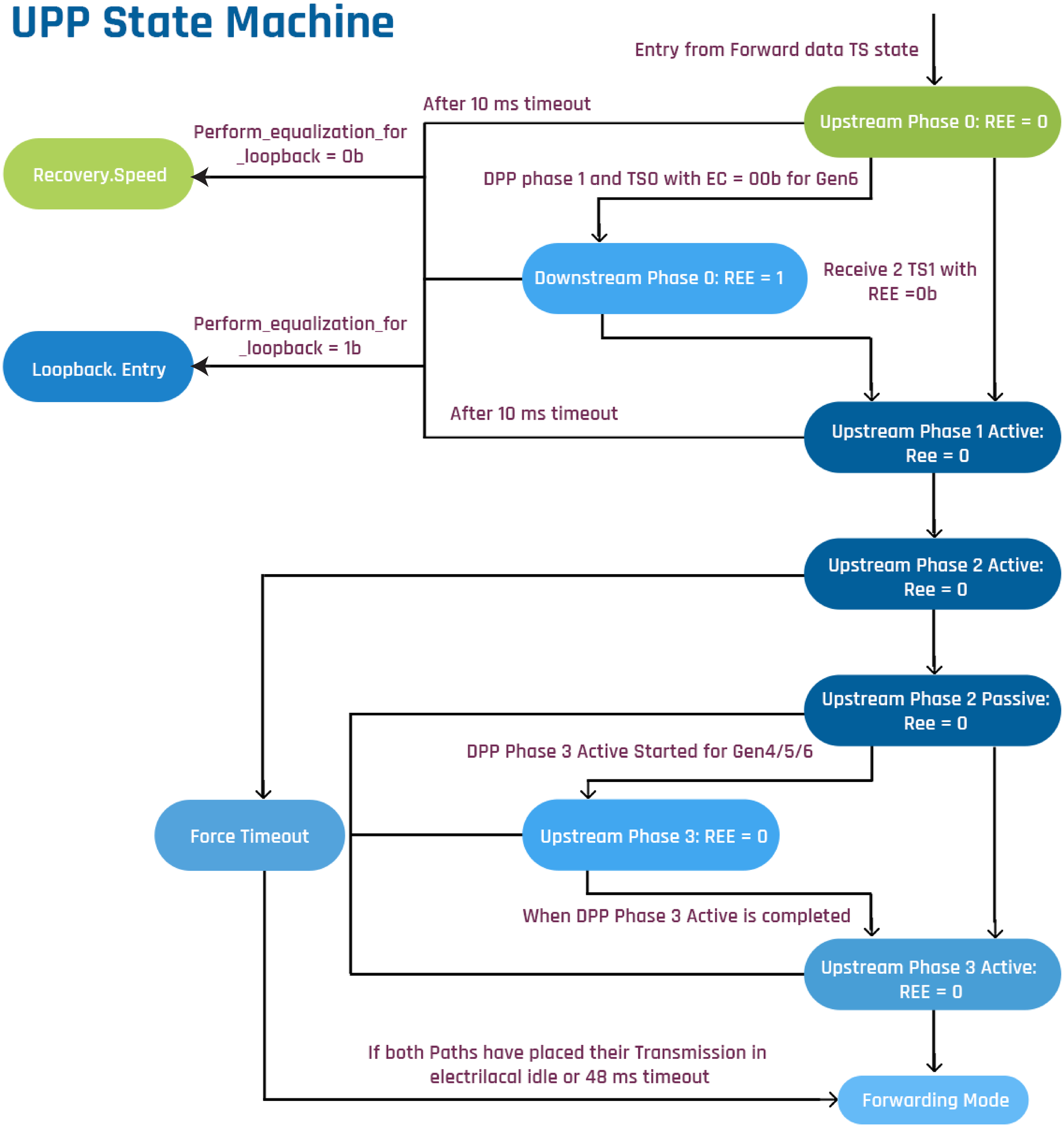
If all configured Lanes receive two consecutive TS1 Ordered Sets with EC=00b then the Retimer switches to Forwarding mode.

Pseudo Port State Machine

DPP State Machine



UPP State Machine



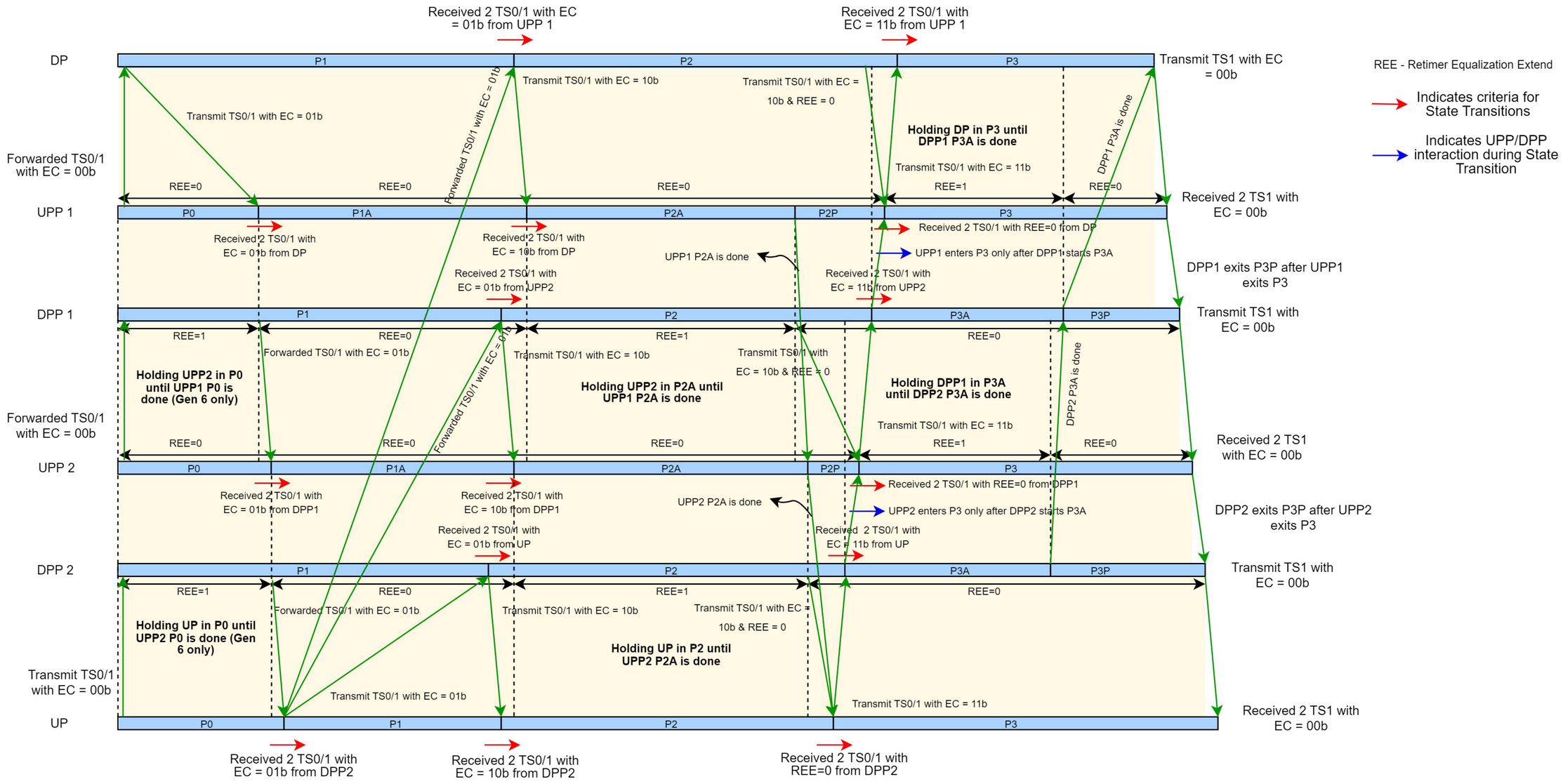
Timing Diagram

Without REE bit present to extend the Equalization, UP enters Phase 3 as soon as Phase 2 is done and sends TS1s prompting DPP to move to Phase 3 Active. So there is a high possibility that UP Phase 3 may get timed out before Phase 3 in DP is done causing the Equalization to fail because both the Equalizations weren't run in sync and didn't get the time it would get when run in sync.

As REE bit is present, DPP can use this to hold UP in Phase 2 until Phase 2 Active of UPP is done and moves Phase 2 Passive.Now UPP moves to Phase 3 along with Phase 3 of DPP, so both UP and DP enter Phase 3 at nearly the same time. Now the chance of UP timing out in Phase 3 is close to zero as the timeout value of Phase 3 in UP is greater than that of Phase 3 in DP.

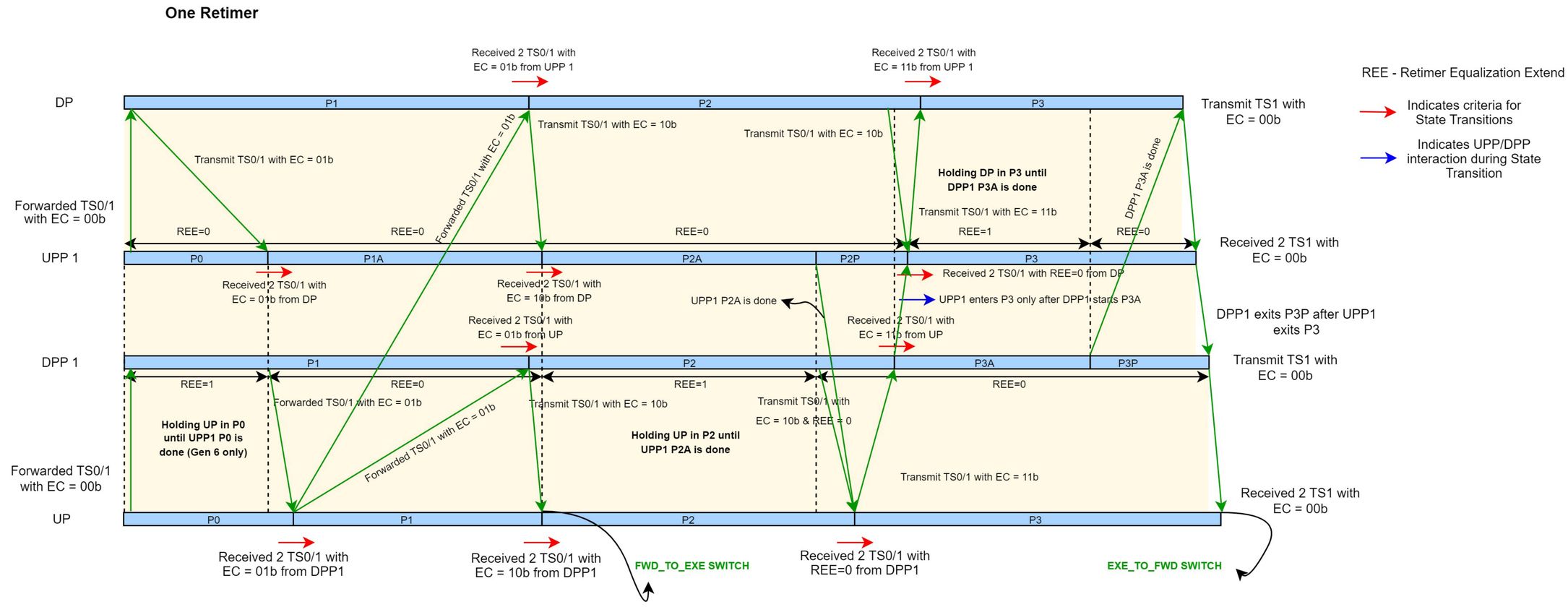
Gen4/5/6

Two Retimers Main



Gen3

One Retimer



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Our engineers have expertise with many high speed protocols and interfaces, including 1G/10G/40G/100G Ethernet, PCIe(Gen1-Gen6), USB3.0/4.0, CPRI/ORAN, DisplayPort, ARINC818 etc.

The team also has deep expertise in Signal processing for wireless and Imaging based solution development, software-defined radio (SDR), as well as encryption, protocol compliance, signal generation, data analysis, IoT technology, and multiple image processing techniques.

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Thank You!

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