Heat Transfer and Flow Simulation in PCB

By:

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Introduction

The loss of heat from the surface of a PCB to the ambient air is difficult to compute as many processes happen at the same time. This situation is much more challenging to describe mathematically since it involves the simultaneous processes of heat spreading by conduction and heat extraction over the surface of the board by convection and radiation. The efficiency of heat transfer from the PCB to air has a significant effect on the temperature difference between the ICs and the air.

There are three basic methods to move heat away from the source, conduction, convection and radiation heat transfer. Conduction is moving the heat through a material (PCB) typically from copper to FR4 to copper and so on. Convection is for removing the heat off the surface material to the air. Radiation is for moving the heat from one surface material to another through air.

Heat Transfer by Conduction:

The general conduction formula for thermal impedance for a given material is:

$$\theta = \frac{L}{K A_{CS}}$$

where,

- $K$ is the Thermal Conductivity Factor
- $L$ is the thermal path length
- $A_{CS}$ is the cross sectional area where the heat is being applied

A low theta is desired since this is the temperature rise in °C per Watt of heat dissipated.

Copper is an excellent thermal conductor. At least one full copper layer is needed to spread the heat. Copper is 1400 times the thermal conductor as FR4.

FR4 is a fairly good thermal conductor (relative to air) through thin layers (perpendicular conduction) but not along the length of the plane’s layer (lateral conduction).

Copper is 9 times better thermal conductor than solder, and solder is 157 times better than FR4

Use Thick Copper and Thin FR4 Layers

Use Multiple Vias to lower the $\theta$ through the PCB (FR4)

Heat Transfer by Convection:

Convection is the method of transfer of heat from the surface of a material to the air. The temperature rise is a function of the power dissipated and inversely proportional to the surface area and the heat transfer coefficient, $h$. The heat transfer coefficient, $h$, is a function of air speed and temperature difference. The range is 7.8 (10°C rise) to 9.1 mW/ (in²-C) (60°C rise), for no air flow.

A conservative value for $h$ is 7.5 mW/ (in²-C) for no air flow.

The temperature rise through convection is given by

$$dT = \frac{P}{hA} = 133 \cdot \frac{P}{A}$$

where,

- $P$ is in Watts
- $h$ is 0.0075 W/(in²-C)
- $A$ is surface area, in². So the thermal impedance is given by $\theta = 1/hA$

Junction Temperature

$T_j = T_{amb} + dT_{pcb-conv} + dT_{pcb-cond} + dT_{jc-ic}$

Heat Transfer by Radiation:

Thermal Radiation is the transfer of heat from one surface to another. It is based on the Stefan-Boltzman Law of Radiation equation and is given by

$$H = \varepsilon \sigma A (T_1^4 - T_2^4)$$
Loss due to Radiation is neglected to allow it to act as factor of safety for PCB Board Components.

Example:

**ESS OF STM 16/64 include :**

1. Two SFP cage (Optical Transceiver) working range  
   -10degC to +85degC  
2. Two Ethernet Phy ICs  
3. Two Artix FPGA and One Kintex FPGA Tj(-40degC to +100degC)  
4. One Microcontroller.  
5. Two SPI Flash, Osc 50 MHz.

Which has to undergo thermal testing as per

1. **Low Temperature (COLD) Cycle:**

   ![Diagram of Low Temperature Cycle]

   - Standard Check
   - Functional check (Equipment should remain operational)
   - Recovery Period, 1 to 2 Hours
   - Rate of change of temperature (1°C/ min)
   - Time taken by the chamber to attain temperature equilibrium

   RH: Not to exceed 50%

   Only Challenge we face is with high temperature cycle

   **Observation:**

   **Preparation** -
   1. SFP+ - Commercial -5 to +70 degC case temperature  
2. Optical Cable - Temperature range not known  
3. Battery RTC - Operational range - -30 to +60 degC  
4. Conformal coating on 2 boards  
5. Motherboard - wires soldered for power input  
6. Air was not coming to our boards. We put tapes in front and bottom to force air in to our boards  
7. Two cards pun in chassis at a time  
8. Optical attenuators seemed loose, they do loose at any time. But looks like once settled they don’t change.

   Tests 1: Cold cycle -
   1. Started from -10 degC. Did functional test. Optical was working  
2. Did standard test at +25 degC. both links worked  
3. At -10 degC ambient temp, FPGA junction temperature was +15 degC

   Test 2: High temperature cycle -
   1. Started with +60 degC and did functional testing. No optical link worked  
2. At +60 degC, one FPGA junction temp was +85degC and 2nd was +88degC
4. At +55 degC, 2nd optical cable did not work

Chassis made by Client -
1. Fans orientation is backward
2. Low power fans so air is not coming to our cards
3. There should be fan tray for forced cooling and some more cutouts on bottom side

**Improvements:**
1. There is a possibility of putting 1U fan tray on bottom of the chassis
2. Can provide cutout on bottom plate.
3. Can put heat sink on SFP+ cages also along with forced cooling
4. There is a possibility that customer may not accept the cards if we put fans on each card. So better to go with fan tray
5. Simulations will be done with following conditions –

**Simulation**
1. with 5 cards

<table>
<thead>
<tr>
<th>Thermodynamic parameters</th>
<th>Static Pressure: 101325.00 Pa</th>
<th>Amb. Temperature: 60.00°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation</td>
<td>FPGA : 6W</td>
<td>SFP : 2W</td>
</tr>
<tr>
<td></td>
<td>Artix : 2W</td>
<td>LPC1788 : 0.2W</td>
</tr>
<tr>
<td></td>
<td>Clock : 0.9W</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Solid parameters</th>
<th>Default material: Aluminum 6061</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Initial solid temperature: 25.00°C</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Fan</th>
<th>5 small fan each of 5 CFM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 fan Tray of 600 CFM</td>
</tr>
</tbody>
</table>

With Power supply cards 70% eff, with 10 cards load 12V output, shared between cards
3. With and Without fan tray
4. By putting different type of heat sink on SFPs and FPGAs
5. With packed top plate and (with holes later)

**Simulation -**
1. with 5 cards

**Conditions & Observation**

Finite Element Analysis essentially consists of the following 3 steps:
- Pre-processing
- Processing or Solution
- Post-processing

The Pre-processing step is, quite generally, described as ‘defining the model’ and it includes the following steps:
1. Define the enclosed (water tight) geometric domain of the problem.
2. Define the element type(s) to be used
3. Define the material properties of the elements
4. Define the geometric properties of the elements
5. Define the element connectivity (mesh the model)
6. Define the physical constraints (boundary conditions)
7. Define the loadings (Volumetric Heat Source, Radiative Surface, Flow Inlet and Outlet)

Once the geometric domain (modelling) of the problem is defined using any CAD application, grid generation is the next process (from Step 2 to Step 5). Once the grid is generated, the model could be taken forward for stress computation.

The pre-processing step is critical. In no case is there a better example of the computer-related axiom “garbage in, garbage out.” A perfectly computed finite element solution is of absolutely no value if it corresponds to the wrong problem. Therefore a high-quality, optimized grid always leads to a high-quality final output.

A very important aspect of meshing a model with elements is to ensure that, in regions of geometric discontinuity, a finer mesh (smaller elements) is defined in the region. This is true in all finite element analyses.
(structural, thermal, and fluid), because it is known that gradients are higher in such areas and finer meshes are required to adequately describe the physical behavior.

Meshing is an essential pre-processing step in Finite Element Analysis. The final solution always depends on the quality of the mesh used during computation. In simple terms, Meshing means breaking up of a physical domain into simpler domains called the elements. Usually there are standard shapes into which the simpler domains are “broken into”. The basic idea of a mesh-generation scheme is to generate element connectivity data and nodal-co-ordinate data by reading in the input data for a few key points.

Commercially many tools are available for Grid generation. Part and assembly modelling, pre-processing, processing and post processing could be performed using all leading CAD tools like Pro-Engineer, Unigraphics, Solidworks, CATIA etc. There are specialised solver tools such as ANSYS, ABAQUS, Msc Nastran etc which could effectively be used for meshing. Apart from these, Hypermesh is another CAE tool, which specialises exclusively in meshing. You can easily checkout most of the tests specified according to JSS 55555 standards for ESS.

Some tools are not efficient in determining the correct scenario while importing PCB parameters. For example; when you are working with Ansys ICEPAK, If you import BRD, you will get only the PCB 3D Model irrespective of trace layer and vias etc., there you will be needing .ART license to fully relate your model to actual PCB, means you need a working Cadence tool in your system. To achieve more accurate results, It is better if you can either relate your ICs (Heat Source) to their respective package (ready to use) provided within the tool (PBGA, Cavity Down BGA, FFBGA, Flip Chip, QFP, QFN, DUAL, Stacked Die, Package On Package) or you can create Delphi model of different ICs or you can directly download thermal model of that ICs provided by manufacturer (Ex. Zyic, Kintex, Artix … by Xilinx).

If your fan is not close enough then try to use radial fin heat sink instead of straight close fins (to allow more air to pass through). Always try to have optimum number of fins.

Use Thermal Pad between Heat Sink and ICs to increase heat transfer through conduction as thermal pad increases contact surface area between the two.

**Post Processing Step or Results**

Colour Legend show the range that particular parameter has changed.

Below is the colored surface plot of solid temperature ranging min to max corresponding blue to red colour.

**Without Fan Tray**

**MAXIMUM TEMPERATURE ACHIEVED:** 123.74 degC

**With Fan Tray**

**MAXIMUM TEMPERATURE ACHIEVED:** 123.74 degC
MAXIMUM TEMPERATURE ACHIEVED: 92.86 degC

With Heat Sink, Modified Chassis & Fan Tray

MAXIMUM TEMPERATURE ACHIEVED: 88.73 degC (FPGA)

The accuracy of the result can vary from practical scenario but it can be assumed as an additional factor of safety. There may be chances of ICs failure due to manufacturing defect (like presence of Hot Spots, etc.) and should be taken into account.